

**32-bit ARM® Cortex-M4F based MCU with LDO,
integrated 3-phase pre-driver with supply up to 28V****Features**

- 32-bit ARM® Cortex-M4F CPU with FPU
 - 100 MHz maximum frequency
 - Memories
 - Up to 128 KB embedded flash
 - Up to 1 KB emulated EEPROM
 - Up to 32 KB on-chip SRAM
 - Power Management
 - Single battery supply from 5.5V to 28V (42V for load dump).
 - Integrated 3.3V and 5V LDO for MCU and main I/O supply
 - Integrated 5V LDO for external sensor
 - Sleep mode and stop mode for power saving
 - POR, Brown-out detector (BOD)
 - Pre-Driver Module
 - 2-Phase/3-Phase Pre-Driver for motor control
 - Integrated charge pump for 100% duty cycle
 - Programmable driving capability up to 300mA
 - Programmable output swing from 8V to 11V
 - Four/Six external power FET V_{DS} monitors
 - Clock
 - Crystal oscillator with both internal oscillator and external clock input support
 - Internal 32MHz factory-trimmed oscillator
 - Internal 32MHz backup-safety oscillator
 - PLL for CPU clock, maximum up to 100MHz
 - 8-channel DMA controller
- 

QFN48 (7 x 7 mm, 0.5mm pitch)
QFN56 (8 x 8 mm, 0.5mm pitch)
- 13-bit A/D converter (up to 9 channels)
 - As low as 200 ns conversion time
 - Single-ended and differential sampling
 - Open/short detection for safety
 - Three temperature sensor
 - 1 x T-sensor for MCU
 - 1 x T-sensor for PMU
 - 1 x T-sensor for LIN transceiver
 - Monitoring ADC (13-bit)
 - Monitor critical voltages
 - Programmable gain amplifier (PGA)
 - One single-ended PGA with gain option:
1, 2, 4, 8, 16, 32, 48, 64
 - One differential PGA with gain option:
2, 4, 8, 16, 24, 32, 48, 64
 - Differential PGA supports -1.5V ~+2V input
 - Analog comparator
 - Two (one pair) high-speed comparators with digital deglitch filter
 - Integrated phase voltage comparison
 - 3-phase voltage sensing and 1-reference sensing
 - 3 dedicate phase comparator
 - Three 10-bit DACs and 1 DAC buffer
 - One D2S (Differential to single-ended) buffer

- LIN transceiver compatible with LIN spec 2.2A and SAEJ2602-2
- 1 input with high voltage monitoring
- PWM
 - Four enhanced PWM modules
 - 8 PWM outputs in total
 - Flexible waveform generation with phase lead/lag control
 - All events can trigger ADC conversion
- Up to 27 GPIO Pins
 - Configurable pull-up/pull-down resistors
 - Programmable digital input deglitch filter
- Enhanced Capture Module (ECAP)
 - Flexible input capture pin
 - Four 32-bit capture registers
 - Capture and APWM mode selection
- Debug mode
- Serial wire (SW) debug & JTAG interfaces
- 6 Timers
 - Three 32-bit general-purpose timers
 - Two 32-bit watchdog timers
 - Sys tick timer 24-bit down-counter
- Communication interfaces
 - UART (with LIN support) x 2, An external LIN PHY required for UART1
 - SPI x 2
 - I2C x 1
 - CAN (with FDCAN support) x 1
- Security Modules
 - 64-bit unique ID, CRC x 1
- Operating temperature
 - Junction temperature: -40 to +125°C.
 - Ambient temperature: -40 to +105°C.
 - Industrial grade

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Revision history

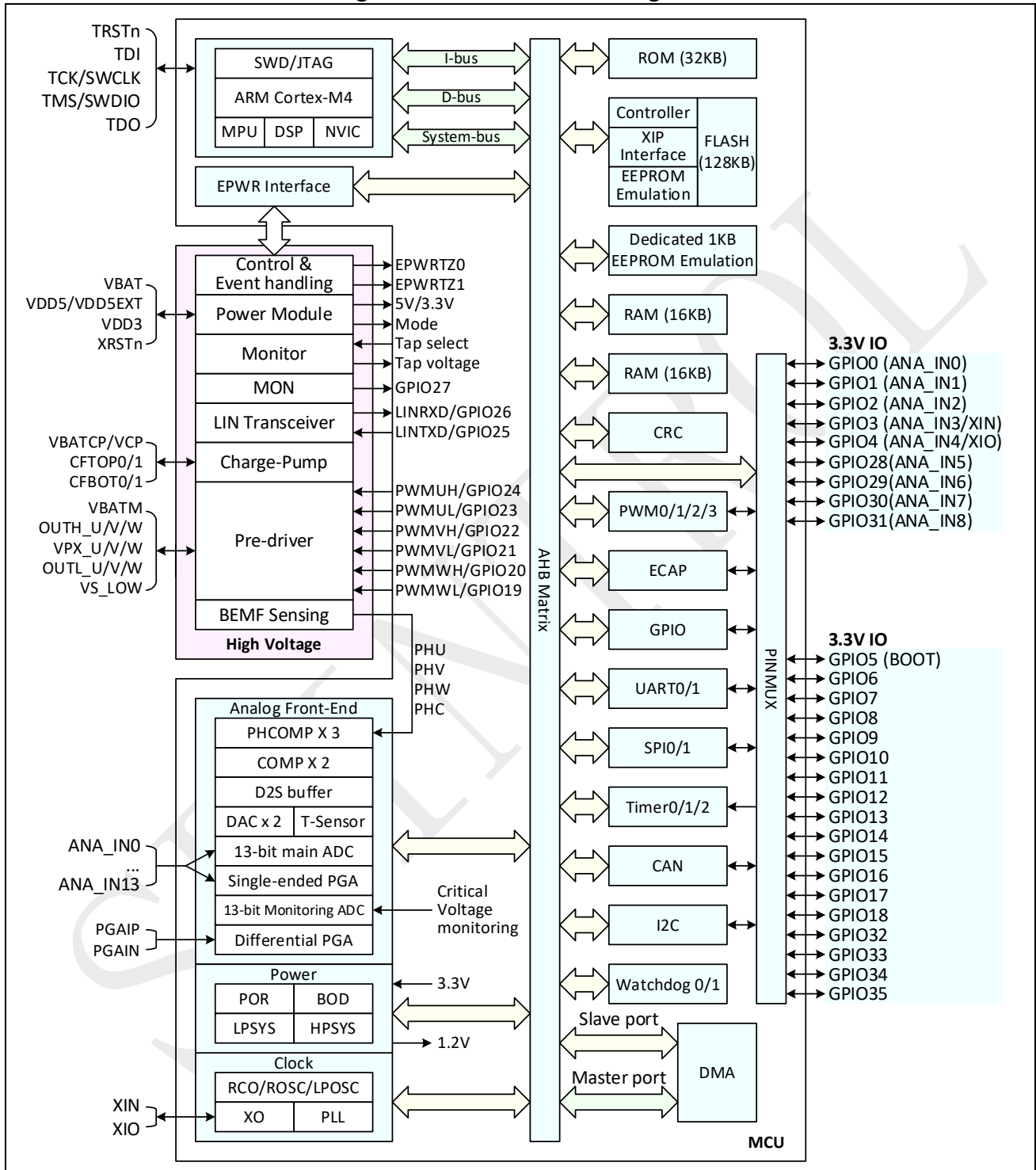
Version	Date	Author	Status	Changes
C/0	2025-01-23	L. Chen	Outdated	1. Initial release.
C/1	2025-05-08	J. Zhou	Outdated	1. Add package information of QFN56. 2. Modify description of I2C mode. 3. Modify value of I_{OH} and I_{OL} in Table 5-2 and Table 5-3 .
C/2	2025-07-02	J. Zhou	Outdated	1. Modify Table 5-15 .
C/3	2026-05-13	J. Zhou	Released	1. Update Table 6-3 and Figure 6-3 . 2. Add Section 6.1.2 . 3. Modify BOD threshold in Section 5.6 . 4. Add Section 5.10 . 5. Update Section 5.7 . 6. Update Table 5-22 . 7. Add Important Statement and Disclaimer.

Terms or abbreviations

Terms or abbreviations	Description
BEMF	Back Electro-Motive Force
DPGA	Differential Programmable Gain Amplifier
SPGA	Single-ended Programmable Gain Amplifier
D2S	Differential to Single-ended

1 Device overview

Figure 1-1: SPD1177 block diagram



The SPD1177 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller. The SPD1177 incorporates a 32-bit ARM® Cortex-M4F high-performance processor with a software-programmable clock rate up to 100 MHz, 32 KB SRAM, 128 KB embedded flash with up to 1 KB EEPROM emulated by extra 12 KB flash, and an extensive range of enhanced I/Os and peripherals. The device offers a 13-bit ADC, one differential PGA and one single-ended PGA, four enhanced PWMs,

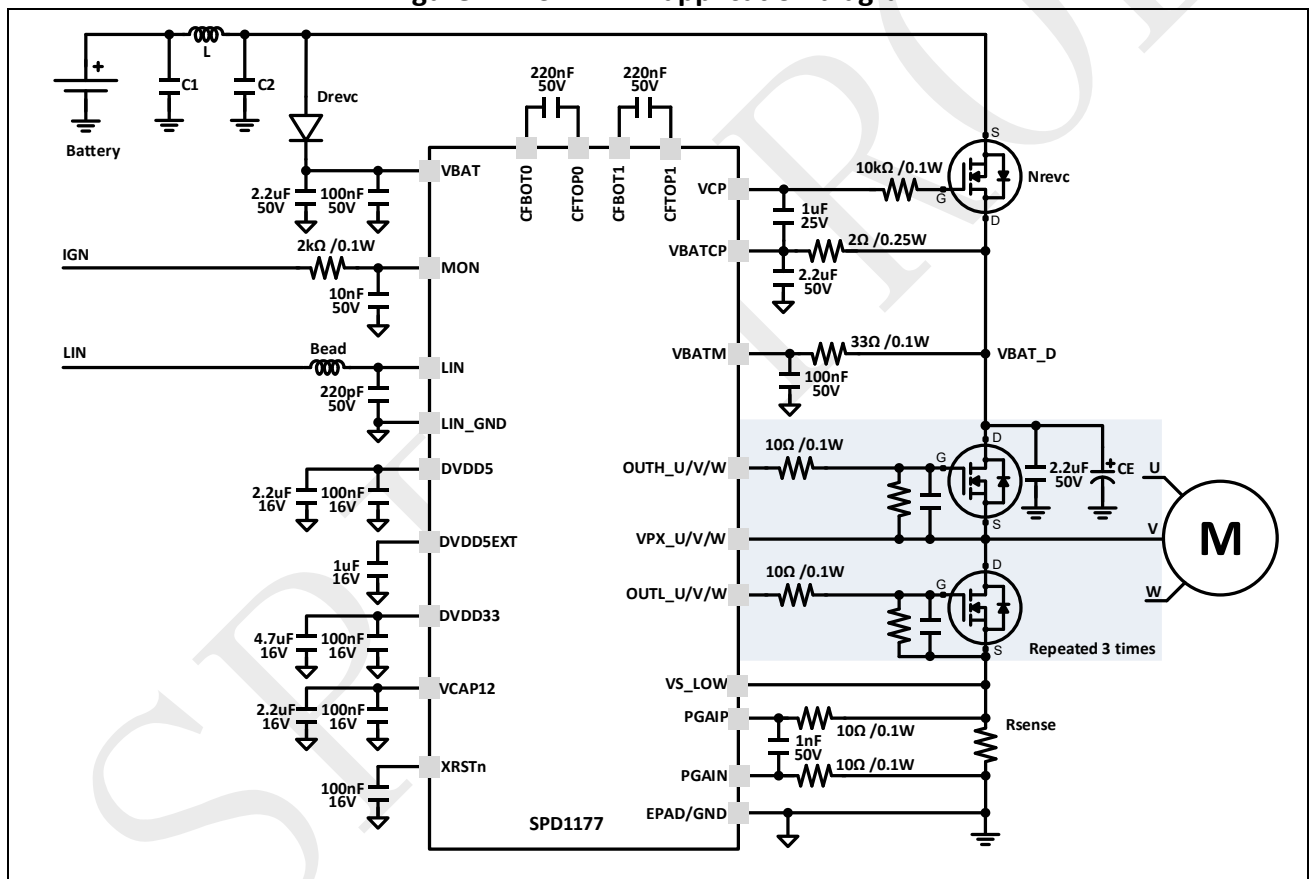
three general-purpose 32-bit timers, as well as standard and advanced communication interface: two UARTs with LIN support, two SPIs, one I2C and one CAN.

The SPD1177 operates with a single power supply from 5.5V to 28V (42V for load dump) and supports stop/sleep mode for power saving. It integrates two 5V LDOs for internal power system and external sensor and integrates 3.3V and 1.2V LDOs for MCU operation. It supports 3.3V I/O for logic and analog input channel. The junction temperature range is from -40 °C to +125 °C. The package type is 48-pin or 56-pin QFN.

The SPD1177 employs function safety features such as backup clocking scheme, watchdog timer interrupt and reset, open/short detection and background critical voltage monitoring. All these features make the SPD1177 ideal for motor control in industrial application.

Figure 1-1 shows the functional block diagram for the SPD1177. Figure 1-2 shows the application diagram.

Figure 1-2: SPD1177 application diagram



2 Feature descriptions

2.1 ARM® Cortex-M4F core

The ARM® Cortex-M4F processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPD1177 integrates a full-feature ARM® Cortex-M4F core that can run up to 100MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Serial wire and JTAG debug port (SWJ-DP)

The embedded ARM® SWJ-DP interface is combined by JTAG and serial wire debug port. They are connected to the external I/O port as shown in [Table 2-1](#). The debug port can be disabled when enabling SPD1177 certain security feature.

Table 2-1: Debug interface definition

Pin Name	Serial wire mode (Disable SWV)	Serial wire mode (Enable SWV)	JTAG mode
GPIO15	User specified function channel	User specified function channel	TDI
GPIO16	User specified function channel	SWV	TDO
GPIO17	SWD	SWD	TMS
GPIO18	SWCK	SWCK	TCK

[1] The purpose of setting GPIO16 through the 24th bit of ARM® Cortex-M4F register (CoreDebug->DEMCR) located at address 0xE000EDFC: 1—SWV output; 0—function specified by user through software.

Note: In debug mode, TRSTn must be tied to the logic high(3.3V).

2.3 Boot ROM

The Boot ROM contains boot code, Flash software library code and emulated EEPROM software library code. User can call these software library to access the Flash memory and the emulated EEPROM directly.

2.4 Embedded SRAM

The SPD1177 has implemented 32 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock frequency with 0 wait states.

2.5 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data. To enhance the lifetime and store critical data, another 12 KB Flash memory is used for EEPROM emulation to support up to 1 KB effective capacity.

2.6 Nested vectored interrupt controller (NVIC)

The SPD1177 embeds a nested vectored interrupt controller able to handle up to 54 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4F) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing

- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.7 External interrupt/event controller

The SPD1177 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.8 Power supply and Reset

The SPD1177 supports single power supply (VBAT) from 5.5V to 28V, which powers internal voltage regulators, analog circuitry on chip and the IOs. In addition, for 42V supply, chip will survive for load dump. There are no special power-up sequence requirements for the SPD1177.

The SPD1177 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.9 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the power supply and different domain power (VBAT/VBATCP/DVDD5/DVDD5EXT/DVDD33/VCAP12) and compare them to the programmable threshold. An interrupt or reset can be generated when voltage of the power domain is above the up-boundary or below the low-boundary. The interrupt service routine then generates a warning message and/or put the MCU into a safe state.

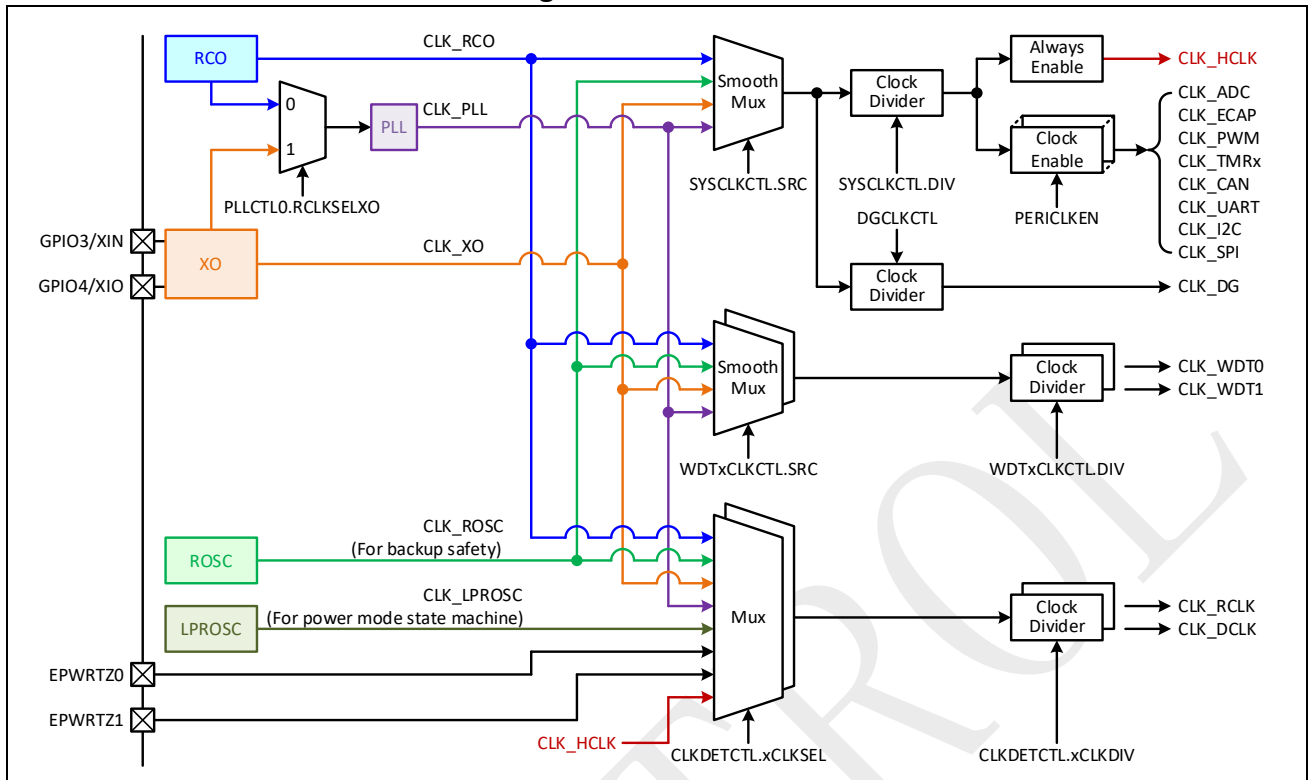
2.10 Clocks

System clock selection is performed on startup. The internal 32 MHz factory-trimmed oscillator is selected by default upon reset. External crystal with frequency from 4MHz to 32MHz can be attached to GPIO3 and GPIO4, so as to generate high precision clock using on-chip crystal oscillation circuits. User can also directly use external clock via GPIO3.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal 32MHz oscillator or external clock as the input reference. The output frequency covers from 25MHz to 100MHz.

Several clock dividers allow the configuration of the AHB, and the peripherals frequency. The maximum allowed frequency is 100MHz. See [Figure 2-1](#) for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 32MHz backup-safety oscillator makes the SPD1177 get rid of clock stuck.

Figure 2-1: Clock tree



2.11 Power management unit

The power management unit generates all the required supplies for the embedded MCU (DVDD5, DVDD33, VCAP12) and external supply (VDD5EXT). The power management system ensures safe behavior of SPD1177 and has a state machine to control power modes transition. The SPD1177 has implemented the power management module with following features:

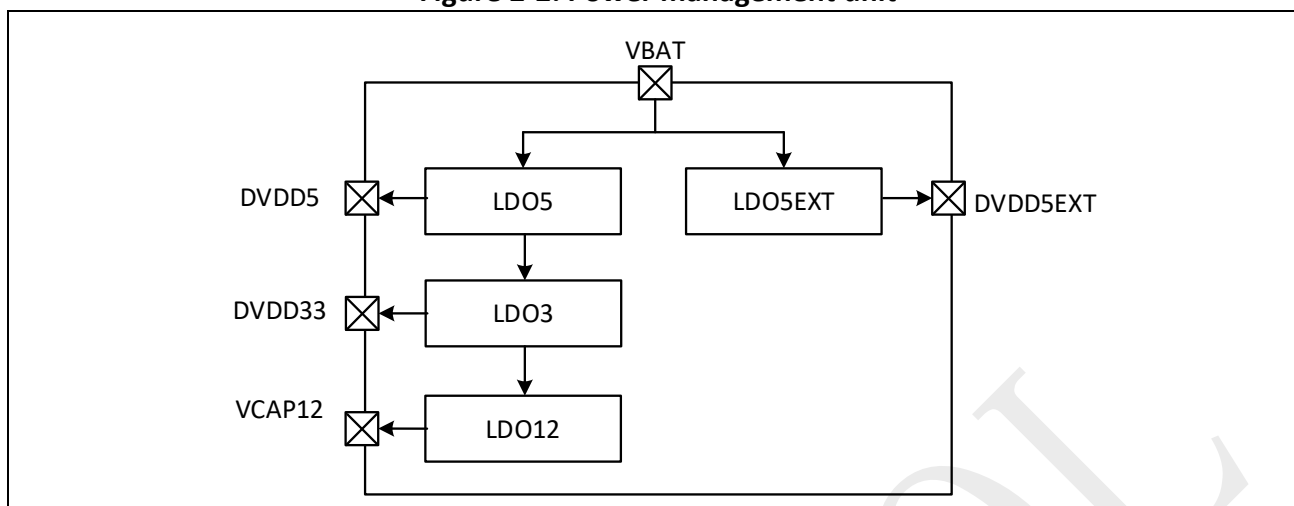
- Support three power modes (active, stop and sleep)
 - Active mode

The voltage regulators (DVDD5, DVDD33, VCAP12) are supplied by on-chip LDO with full current driving capability. All clocks are enabled per user's setup in register control bits.
 - Stop mode

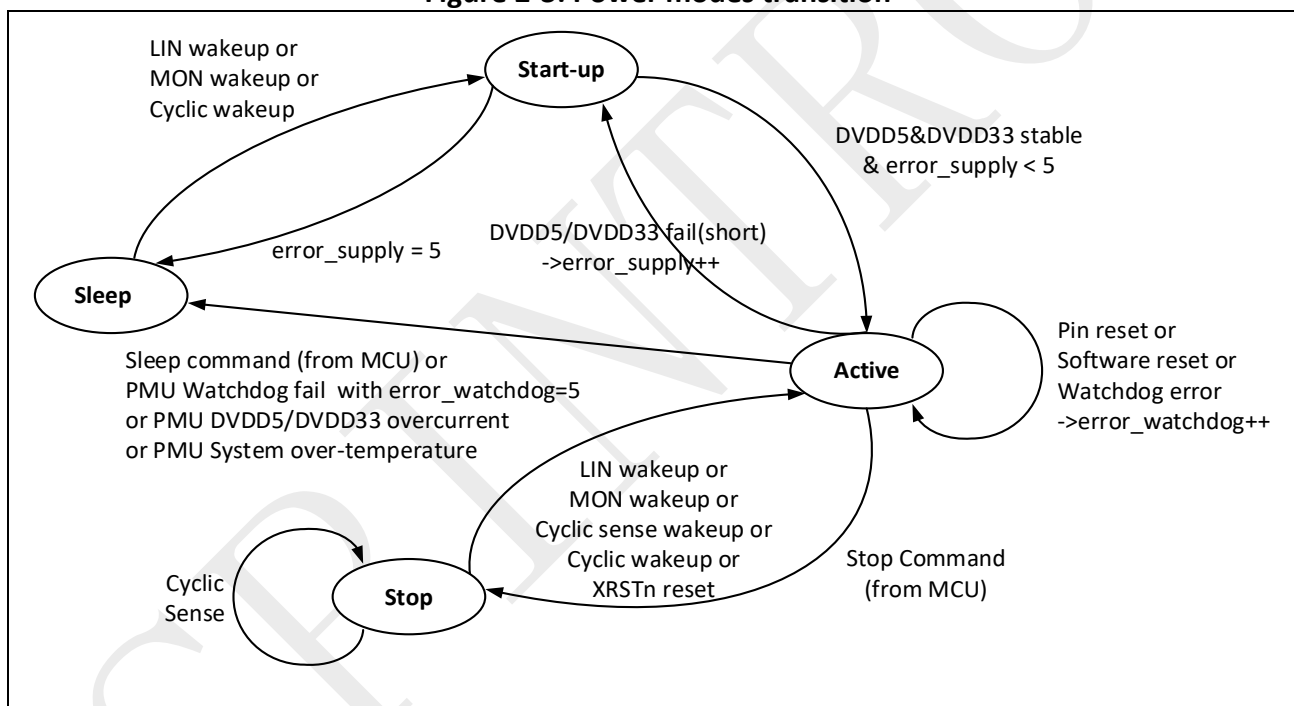
All clocks are stopped except for the 100 KHz clock for power mode state machine. DVDD5, DVDD33, VCAP12 are supplied by low-power LDO with limited current driving capability. VCAP12 can be configured to be below 1.2V to further reduce the static current. All registers and memories retain the content. The system can be waken-up by different wake-up sources, like XRSTn, LIN, MON, cyclic-wakeup and cyclic-sense-wakeup by any GPIO per user's setup with programmable input levels. The CPU will continue to run the instructions when it exit stop mode (XRSTn wake-up will trigger system reset).
 - Sleep mode

The voltage regulators (DVDD5, DVDD33, VCAP12) are totally shutdown. It can be waken-up by LIN/MON/cyclic-wakeup and the whole system will go through a cold start-up.
- The voltage regulators (DVDD5, DVDD33, VCAP12 and VDD5EXT) supports over-current, over/under-voltage protection
- Provide over-temperature protection
- Configurable wakeup sources (LIN, MON, cyclic wakeup, cyclic sense wakeup, GPIOs)

The power system diagram is shown in [Figure 2-2](#).

Figure 2-2: Power management unit

The three power modes transition is shown in [Figure 2-3](#).

Figure 2-3: Power modes transition

2.12 DVDD5 LDO

The DVDD5 LDO provides power for 5V domain functions. The SPD1177 has implemented a DVDD5 LDO module with following features:

- 5V LDO with 90mA driving ability
- Overcurrent monitoring and self-shutdown
- Pre-regulator for DVDD33 LDO
- Pull down current source (typically 1mA) at the output for sleep mode only

2.13 DVDD33 LDO

The DVDD33 LDO provides power for 3.3V domain functions. The SPD1177 has implemented a DVDD33 LDO module with following features:

- 3.3V LDO with 60mA driving ability

- Overcurrent monitoring and self-shutdown
- Pre-regulator for VCAP12 LDO
- Pull down current source (typically 5mA) at the output for sleep mode only

2.14 DVDD5EXT LDO

The DVDD5EXT LDO provides power for external circuits. The SPD1177 has implemented a DVDD5EXT LDO module with following features:

- 5V LDO with 40mA driving ability
- Overcurrent monitoring and self-shutdown
- Pull down current source (typically 1mA) at the output for sleep mode only.

2.15 VCAP12 LDO

The VCAP12 LDO provides power for the embedded MCU. The SPD1177 has implemented a VCAP12 LDO module with following features:

- 1.2V LDO with 40mA driving ability

2.16 Power tracking amplifier

Power tracking amplifier buffers critical power signals to the 13-bit Monitoring ADC, to monitor power status. The critical power signals sent to the 13-bit Monitoring ADC are VBAT, VCP, VMON, VDD5, power bandgap, PMU temperature sensor voltage and LIN temperature sensor voltage.

2.17 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM.

- If GPIO5 is high upon power-on reset, XRSTn pin reset or the system reset request from the ARM® Cortex-M4F, ISP boot mode is entered. The boot loader reprograms the embedded Flash by using UART or LIN interface. When UART interface is used, GPIO10 is configured as UART0_TXD and the GPIO11 is configured as UART0_RXD.
- For all other cases, the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000.

2.18 General-purpose IOs (GPIOs)

The SPD1177 can be configured to support as many as 27 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter
- Pure 3.3V I/O capability multiplexed with ADC input channel for GPIO0~GPIO4, GPIO28 ~ GPIO31
- Full 3.3V I/O capability for GPIO5 ~ GPIO18, GPIO32 ~ GPIO35

2.19 General Purpose Timers

The SPD1177 includes three identical general-purpose timers, which features:

- Independent clock enable control
- 32-bit auto-reload down-counter
- Generate interrupt request, ADCSOC event and PWMSYNC event when the counter reaches zero

- Support 4 modes
 - General timer: Periodic down-counter
 - Gated timer: Down-counter enabled by external input level
 - Event counter: Down-counter upon external input edge
 - Event capture: Down-counter with timestamp latched upon external input edge

2.20 Watchdog timer

The SPD1177 implements two identical watchdogs, which features:

- Independent clock source, clock dividing and clock enable control
- 32-bit auto-reload down-counter
- Generate interrupt request when the counter reaches zero
- Generate reset request when the counter reaches zero and the interrupt flag is already set
- Can be frozen or free-running in debug mode

2.21 SysTick timer

There is a SysTick timer embedded in the ARM® Cortex-M4F. It is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter with auto-reload capability
- Maskable system interrupt generation when the counter reaches 0

2.22 UART

The SPD1177 has two UART modules that are functionally compatible with the 16550A and 16750 industry standards. They features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 6.25 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

Specific hardware is also implemented to enable LIN features:

- Compatibility with LIN 2.2 protocols
- Configurable baud rate up to 20 kbps
- Identification masks for message filtering
- Hardware processing on break field, sync byte field, protected ID field, data field and checksum field
- Response length can be defined by bit 5 and bit 4 of protected ID field, or by register control
- Programmable classic checksum mode or enhanced checksum mode

2.23 I²C

The I²C bus interface complies with the common I²C protocol. It features:

- Four speeds: Standard mode (100 kb/s), Fast mode (400 kb/s), Fast mode plus (1 Mb/s) and High-Speed mode (3.4 Mb/s)
- Clock synchronization
- Master or slave I²C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.24 SPI

SPD1177 includes two SPI modules, which allow half/full-duplex, synchronous, serial communication with external devices. They features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- Local clock divider for flexible communication speed control, with up to 50 Mbps capability
- MSB-first data order
- Programmable clock polarity and phase
- 16 x 32-bit deep transmit and receive FIFOs, respectively

2.25 CAN

The SPD1177 has implemented one CAN module. It is used for communication based on CAN protocol. An external CAN transceiver is required for the connection to the physical layer (CAN bus). The CAN module features:

- Compatible with ISO-11898-1:2015 specification, whose frame format is called classical CAN and ISO-FDCAN.
- Compatible with Bosch CAN2.0B specification.
- Compatible with Bosch FDCAN V1.0 specification, whose frame format is called NONISO-FDCAN.
- Support Bus-Off recovery.
- Support automatic message re-transmission after transmission failure.
- Support restricted mode.
- Support monitor mode.
- Support test mode.
- Support 64 mailboxes with independent message identifier mask for each mailbox.
- Support automatic remote frame handling.
- Support CAN bus error recording.
- Support 32-bit timestamp.

Note: The CAN module of SPD1177 does not support wake-up function, users need to select a CAN PHY that supports wake-up function and connect the CAN PHY wake-up signal to the MON pin or GPIO pin of SPD1177 to realize the CAN wake-up function.

2.26 ADC

One 13-bit analog-to-digital convert is embedded into SPD1177 and has up to nine external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has built-in sample-and-hold (S/H) with two input channels, which is suitable for differential sampling. The start of sample and conversion can be triggered by the software, the internally connected hardware event signals from the general-purpose timers and the PWM outputs, or from the external pin input.

The 13-bit ADC features:

- 200 ns minimum conversion time and independent configurable sampling time
- Support single-ended or differential sampling
- Full range analog input: 0 V to 3.65 V
- Input open and short detection for safety

Another 13-bit ADC (Monitoring ADC) is provided to routinely check critical voltages below per user's request for system safety concern. An interrupt can be generated if the monitoring item is out of the pre-defined range.

Please see [Table 5-19](#) for 13-bit ADC characteristics and [Table 5-20](#) for Monitoring ADC characteristics.

2.27 Temperature sensor

SPD1177 includes three temperature sensors. One for MCU, one for PMU in high voltage and one for LIN transceiver. Their sensing voltages vary linearly with temperature. These sensing signals are internally connected to the input channel of monitoring ADC, which is used to convert the sensor output voltage into a digital value.

2.28 PGAs

SPD1177 includes a differential programmable gain amplifier (DPGA) with two dedicated pins. It features:

- Programmable gains: 2, 4, 8, 16, 24, 32, 48 and 64
- Differential input voltage: $\pm 2.7/\text{PGA_Gain}$
- Wide common mode input range: -1.5V ~ 2V with Gain 2x
- Settling time: 250 ns to 1.4 μ s

A single-ended PGA (SPGA) is also implemented in SPD1177. The four external ADC input channels (ANA_IN0~ANA_IN3), the temperature sensor output, and internal 1.2V power can be selected as the SPGA input. It features:

- Programmable gains: 1, 2, 4, 8, 16, 32, 48 and 64
- Settling time: 300 ns to 2 μ s

Both the outputs from the differential PGA (DPGA) and the single-ended PGA (SPGA) can be selected as the 13-bit ADC input. Please see [Table 5-22](#) for DPGA characteristics and [Table 5-23](#) for SPGA characteristics.

2.29 Analog comparators

The SPD1177 has two high-speed comparators. They are used with two internal 10-bit DAC as reference for monitoring PGA inputs or outputs to check whether the voltage is too high or too low. The comparator output is routed to the PWM Trip-Zone modules.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter

Please see [Table 5-24](#) and [Table 5-26](#) for analog comparator and DAC characteristics.

2.30 Phase comparators

SPD1177 include 3 high speed rail-to-rail phase comparators, which can compare three phases voltage (PHU/PHV/PHW) to the common mode voltage (PHC). Phase comparator has 8-to-1 input mux, it can also used as normal comparator to compare analog ADC input to reference voltage (ADC input or DAC output).

Based on the intrinsic characteristic of motor operation, hardware post-processing is implemented to the comparator output as below, so as to simplify user's software.

- Blanking with programmable window size
- Filtering with programmable window size
- Finite state machine (FSM) to ignore the systematic false alarm due to the large interferences via motor toggling. The FSM can be reset to initial state per user's software. The first zero-crossing event after the FSM reset is ignored.

2.31 DAC and DAC buffer

The SPD1177 has three 10-bit DAC, which can generate a voltage from 0 to VDDA. DAC0 and DAC1 can be used as too high or too low reference for comparators. DAC2 can be used as the reference of phase comparator.

The SPD1177 has one DAC buffer, it can select DAC0 or DAC1 as its input, and send output through ANA_IN2 pin.

2.32 D2S buffer

The SPD1177 integrates one D2S (differential to single-ended) buffer, which can convert DPGA's differential output voltage to single-ended output voltage and sent it to ANA_IN4 pin. Through external RC filter (typically, $R = 1k\Omega$, $C = 1\mu F$), the single-ended output voltage can be sent back to ANA_INx ($x = 0 \sim 3$) pin and measured by 13-bit ADC. D2S buffer gain is fixed at 0.5.

2.33 PWMs

The SPD1177 integrates four PWM modules and supports six PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion

- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.34 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPD1177 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.35 Cyclic redundancy check (CRC)

The SPD1177 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 2^{32} byte length for CRC calculation
- Eight CRC standard polynomials supported

2.36 Pre-Driver System

Pre-Driver system consists of a two/three low-side and high-side pre-drivers which can drive the two/three phases of low-side and high-side external power NFET's. The SPD1177 has implemented this Pre-Driver system with following features:

- Embedded dual charge pump guarantees 100% duty cycle
- High performance down to 5.5V supply
- Built in non-overlap time to prevent crow-bar current even in case of input PWM overlapping
- Dynamically adjustable Pre-Driver charge/discharge strength to optimize switching and EMI
- VDS monitors for short circuit detection in on- and off-state

2.37 LIN transceiver

The local interconnect network (LIN) module is a serial communication protocol designed to support automotive networks in conjunction with controller area network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The SPD1177 has implemented an LIN module (connected to UART1 internally) with following features:

- Operational with VBAT 7.0 to 18 V DC, functional up to 28 V and down to 5.5V. For load dump, VBAT can survive up to 42V.
- Support 2 transmission modes 10.4kBaud/20kBaud, functional download with 76.8kBaud
- Integrated 30kΩ termination resistor for slave applications
- Compatible with LIN protocol specification 2.2, and SAEJ2602-2
- Low standby current in Sleep mode
- Over-temperature protection
- TxD timeout feature (optional, enabled by default)
- Very high immunity against electromagnetic interference

2.38 High voltage monitor

The high voltage monitor (MON) module is dedicated to monitor external high voltage levels above or below a specified threshold (normally is $V_{BAT}/2$). Its output can be used as a digital level from high voltage pin or used to detect a wake-up event at the high-voltage MON pin in low-power mode.

The SPD1177 has implemented an MON module with following features:

- High voltage input with $V_{BAT}/2$ threshold voltage
- Integrated pull-up and pull-down current sources with automatic selectable capability
- Wake-up event for power saving modes
- Level shift from high voltage pin to low voltage domain

2.39 BEMF sensing

The back electromotive force (BEMF) sensing module is used to detect zero crossing events, which can be used as a commutation trigger for BLDC applications.

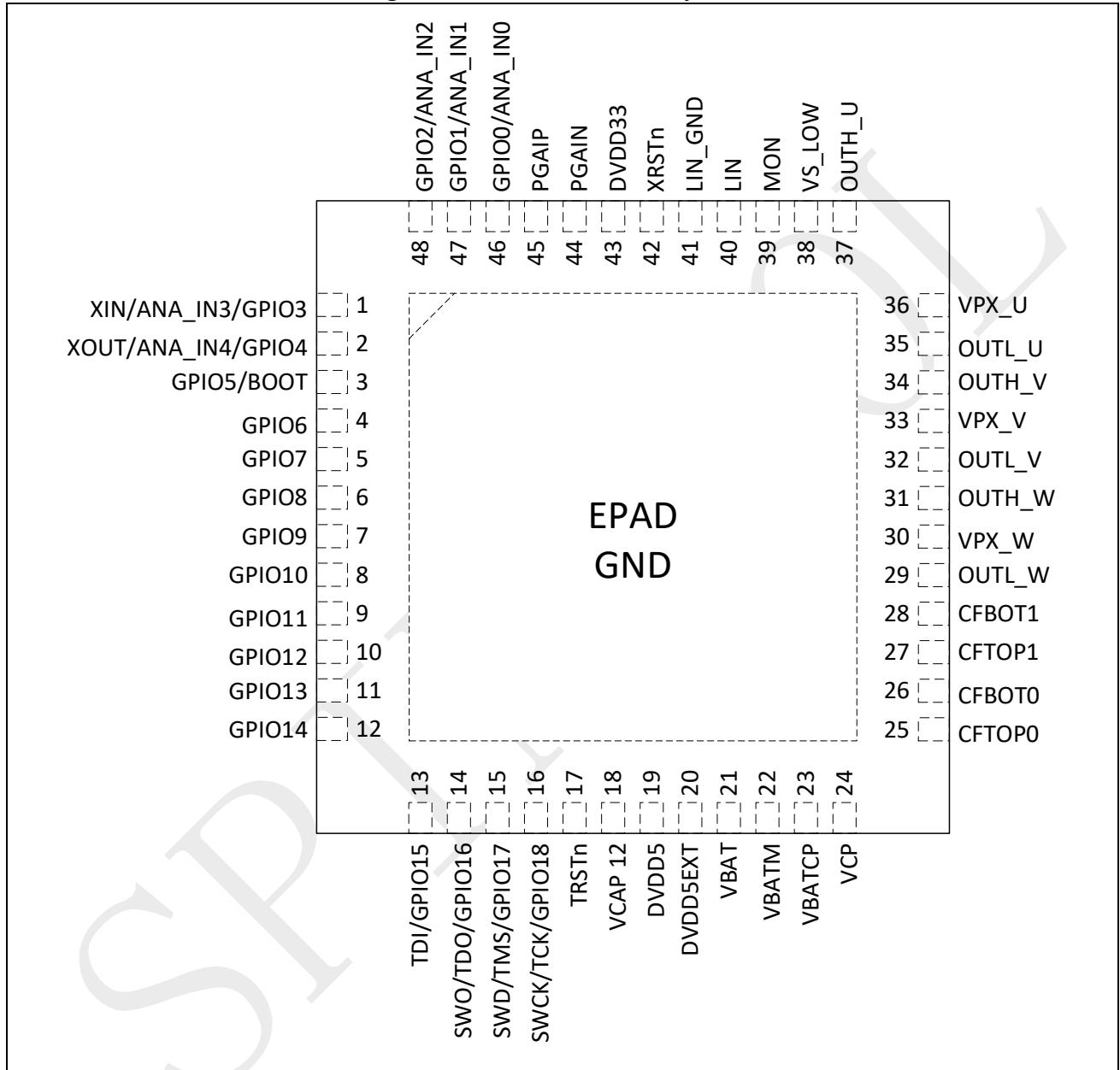
The SPD1177 has implemented a BEMF sensing module with following features:

- Implement U/V/W phase zero crossing detect
- BEMF detection scheme with the virtual neutral point

3 Pinout and pin description

3.1 QFN48

Figure 3-1: SPD1177 QFN48 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in [Table 2-1](#).

Table 3-1: SPD1177 QFN48 pin definitions

Pin	Type	Signal	Sub-Type ^[1]	Description
1	3.3V I/O	GPIO3	I/O	General-purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
		XIN	AI	External oscillator input
		COMP_MON0	O	Comparator output monitor 0
2	3.3V I/O	GPIO4	I/O	General-purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
		XOUT	O	External oscillator output
		COMP_MON1	O	Comparator output monitor 1
3	I/O	GPIO5 (BOOT)	I/O	General-purpose input/output 5 (BOOT)
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ00 or EPWRTZ10.
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		ECAP_APWMO	O	APWM mode output of the ECAP
4	I/O	GPIO6	I/O	General-purpose input/output 6
		SPI0_SCLK	I/O	SPI0 clock input/output
		UART1_TXD	O	UART1 transmitted data
		COMP_MON2	O	Comparator output monitor 2
5	I/O	GPIO7	I/O	General-purpose input/output 7
		SPI0_SFRM	I/O	SPI0 frame signal input/output
		UART1_RXD	I	UART1 received data
		COMP_MON3	O	Comparator output monitor 3
6	I/O	GPIO8	I/O	General-purpose input/output 8
		SPI0_MOSI	I/O	SPI0 master output, slave input
		CAN_TXD	I/O	SPI0 master input, slave output
		COMP_MON4	O	Comparator output monitor 4
7	I/O	GPIO9	I/O	General-purpose input/output 9
		SPI0_MISO	I/O	SPI0 master input, slave output
		CAN_RXD	I/O	SPI0 master output, slave input
		COMP_MON5	O	Comparator output monitor 5
8	I/O	GPIO10	I/O	General-purpose input/output 10

Pin	Type	Signal	Sub-Type ^[1]	Description
		UART0_TXD	O	UART0 transmitted data
		PWM0A	O	PWM0 output A
		I2C_SCL	I/O	I2C clock
9	I/O	GPIO11	I/O	General-purpose input/output 11
		UART0_RXD	I	UART0 received data
		PWM0B	O	PWM0 output B
		I2C_SDA	I/O	I2C data
10	I/O	GPIO12	I/O	General-purpose input/output 12
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWM1A	O	PWM1 output A
		PWM3A	O	PWM3 output A
11	I/O	GPIO13	I/O	General-purpose input/output 13
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWM1B	O	PWM1 output B
		PWM3B	O	PWM3 output B
12	I/O	GPIO14	I/O	General-purpose input/output 14
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWM2A	O	PWM2 output A
		I2C_SCL	I/O	I2C clock
13	I/O	GPIO15	I/O	General-purpose input/output 15
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWM2B	O	PWM2 output B
		I2C_SDA	I/O	I2C data
		TDI	I	JTAG data input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
14	I/O	GPIO16	I/O	General-purpose input/output 16
		UART1_TXD	O	UART1 transmitted data
		CAN_TXD	O	CAN transmitted data
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		TDO/SWO	O	JTAG data output or Asynchronous TRACE output
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
15	I/O	GPIO17	I/O	General-purpose input/output 17

Pin	Type	Signal	Sub-Type ^[1]	Description
		UART1_RXD	I	UART1 received data
		CAN_RXD	I	CAN received data
		SPI1_SCLK	I/O	SPI1 clock input/output
		TMS/SWD	I/O	JTAG mode select or SWD data
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
16	I/O	GPIO18	I/O	General-purpose input/output 18
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		PWMSYNCO	O	PWMSYNC output
		ECAP_APWMO	O	APWM mode output of the ECAP
		TCK/SWCK	I	JTAG clock or SWD clock
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
17	I/O	TRSTn	I	JTAG reset pin, reset the JTAG when low
18	1.2V Power	VCAP12	P	1.2 V power Add 2.2uF and 0.1uF bypass ceramic cap to GND
19	5V Power	DVDD5	P	5 V digital power Add 2.2uF and 0.1uF bypass ceramic cap to GND
20	5V Power	DVDD5EXT	P	5 V power for external loading Add 2.2uF bypass ceramic cap to GND
21	HV Power	VBAT	P	High voltage power from 5.5V to 42V Add 2.2uF and 0.1uF bypass ceramic cap to GND
22	HV Power	VBATM	P	High voltage power for vds monitor from 5.5V to 42V Add 0.1uF bypass ceramic cap to GND. Series 33 Ohm resistor from VBAT_D (VBAT for driver).
23	HV Power	VBATCP	P	High voltage power for charge-pump from 5.5V to 42V Add 2.2uF bypass ceramic cap to GND. Series 2 Ohm resistor from VBAT_D (VBAT for driver).
24	HV Power	VCP	P	Charge-pump output voltage, maximum up to 48V.

Pin	Type	Signal	Sub-Type ^[1]	Description
				Add 2.2uF ceramic cap to VBAT_CP .
25	HV Power	CFTOP0	P	Charge pump flying capacitor 0 top plate voltage Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0
26	HV Power	CFBOT0	P	Charge pump flying capacitor 0 bottom plate voltage Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0
27	HV Power	CFTOP1	P	Charge pump flying capacitor 1 top plate voltage Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1
28	HV Power	CFBOT1	P	Charge pump flying capacitor 1 bottom plate voltage Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1
29	HV IO	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive
	-	NC	-	Not connected
30	HV Power	VPX_W	P	Pre-Driver W-Phase power FET switching node
	-	NC	-	Not connected
31	HV IO	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive
	-	NC	-	Not connected
32	HV IO	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
33	HV Power	VPX_V	P	Pre-Driver V-Phase power FET switching node
34	HV IO	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive
35	HV IO	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
36	HV Power	VPX_U	P	Pre-Driver U-Phase power FET switching node
37	HV IO	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
38	Ground	VS_LOW	G	Pre-Driver low side ground
39	HV IO	MON	I	High voltage input for level monitor
40	HV IO	LIN	I/O	LIN bus interface, can be set as input or output.
41	HV Power	LIN_GND	P	LIN bus ground
42	5V I/O	XRSTn	I	Device reset pin, reset the device when low

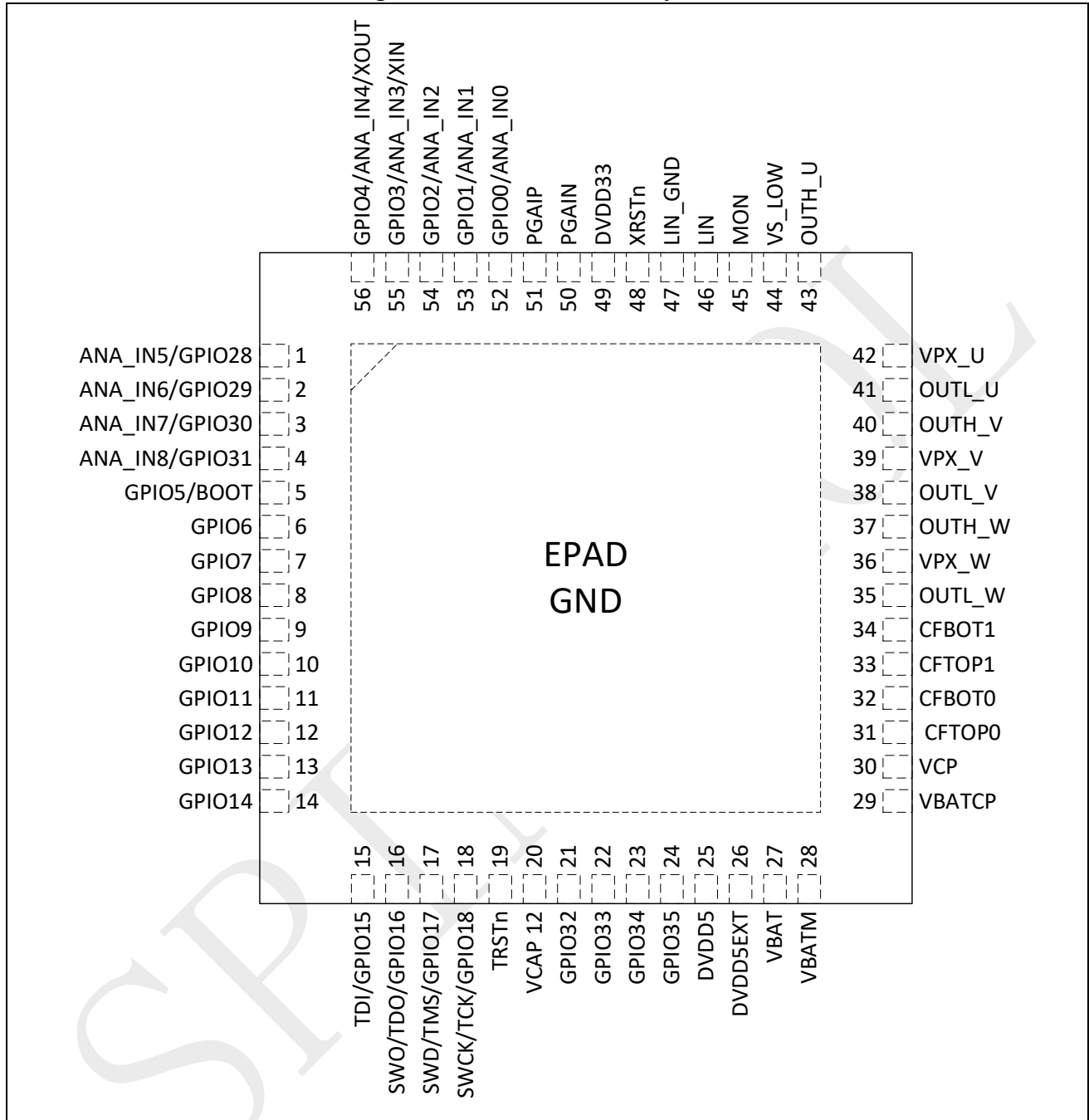
Pin	Type	Signal	Sub-Type ^[1]	Description
43	3.3V Power	DVDD33	P	3.3 V digital power Add 4.7uF and 0.1uF bypass ceramic cap to GND
44	-2V ~ 3.3V input	PGAIN	AI	Differential PGA negative input
45	-2V ~ 3.3V input	PGAIP	AI	Differential PGA positive input
46	3.3V I/O	GPIO0	I/O	General-purpose input/output 0
		ANA_IN0	AI	Analog input channel 0
		PWMSOCAO	O	PWMSOCA output
		PWMSOCCO	O	PWMSOCC output
47	I/O	GPIO1	I/O	General-purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
		PWMSOCB	O	PWMSOCB output
		ECAP_APWMO	O	APWM mode output of the ECAP
48	I/O	GPIO2	I/O	General-purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
		DCLK	O	Clock output from CLKDET module for monitoring
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.
EPAD	Ground	GND	G	Exposed pad, connect to ground

[1] I = digital input, O = digital output or High-Voltage module output, AI = analog input, AO = analog output, P = power supply, G = ground.

[2] **All GPIO pins can be configured as ECAP input.**

3.2 QFN56

Figure 3-2: SPD1177 QFN56 pinout



[1] The figure above shows top view for the package.

[2] When TRSTn is high, GPIO15 ~ GPIO18 may be used for debug interface as shown in [Table 2-1](#).

Table 3-2: SPD1177 QFN56 pin definitions

Pin	Type	Signal	Sub-Type ^[1]	Description
1	3.3V I/O	GPIO28	I/O	General-purpose input/output 28
		ANA_IN5	AI	Analog input channel 5
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWMSOCAO	O	PWMSOCA output
2	3.3V I/O	GPIO29	I/O	General-purpose input/output 29
		ANA_IN6	AI	Analog input channel 6
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWMSOCBO	O	PWMSOCB output
3	3.3V I/O	GPIO30	I/O	General-purpose input/output 30
		ANA_IN7	AI	Analog input channel 7
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWMSOCCO	O	PWMSOCC output
4	3.3V I/O	GPIO31	I/O	General-purpose input/output 31
		ANA_IN8	AI	Analog input channel 8
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWMSYNCO	O	PWMSYNC output
5	I/O	GPIO5 (BOOT)	I/O	General-purpose input/output 5 (BOOT)
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZO0 or EPWRTZ10.
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		ECAP_APWMO	O	APWM mode output of the ECAP
6	I/O	GPIO6	I/O	General-purpose input/output 6
		SPIO_SCLK	I/O	SPIO clock input/output
		UART1_TXD	O	UART1 transmitted data
		COMP_MON2	O	Comparator output monitor 2
7	I/O	GPIO7	I/O	General-purpose input/output 7
		SPIO_SFRM	I/O	SPIO frame signal input/output
		UART1_RXD	I	UART1 received data
		COMP_MON3	O	Comparator output monitor 3
8	I/O	GPIO8	I/O	General-purpose input/output 8
		SPIO_MOSI	I/O	SPIO master output, slave input
		CAN_TXD	O	SPIO master input, slave output
		COMP_MON4	O	Comparator output monitor 4
9	I/O	GPIO9	I/O	General-purpose input/output 9
		SPIO_MISO	I/O	SPIO master input, slave output
		CAN_RXD	I	SPIO master output, slave input
		COMP_MON5	O	Comparator output monitor 5
10	I/O	GPIO10	I/O	General-purpose input/output 10
		UART0_TXD	O	UART0 transmitted data
		PWM0A	O	PWM0 output A
		I2C_SCL	I/O	I2C clock
11	I/O	GPIO11	I/O	General-purpose input/output 11

Pin	Type	Signal	Sub-Type ^[1]	Description
		UART0_RXD	I	UART0 received data
		PWM0B	O	PWM0 output B
		I2C_SDA	I/O	I2C data
12	I/O	GPIO12	I/O	General-purpose input/output 12
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWM1A	O	PWM1 output A
		PWM3A	O	PWM3 output A
13	I/O	GPIO13	I/O	General-purpose input/output 13
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWM1B	O	PWM1 output B
		PWM3B	O	PWM3 output B
14	I/O	GPIO14	I/O	General-purpose input/output 14
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWM2A	O	PWM2 output A
		I2C_SCL	I/O	I2C clock
15	I/O	GPIO15	I/O	General-purpose input/output 15
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWM2B	O	PWM2 output B
		I2C_SDA	I/O	I2C data
		TDI	I	JTAG data input
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
16	I/O	GPIO16	I/O	General-purpose input/output 16
		UART1_TXD	O	UART1 transmitted data
		CAN_TXD	O	CAN transmitted data
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		TDO/SWO	O	JTAG data output or Asynchronous TRACE output
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
17	I/O	GPIO17	I/O	General-purpose input/output 17
		UART1_RXD	I	UART1 received data
		CAN_RXD	I	CAN received data
		SPI1_SCLK	I/O	SPI1 clock input/output
		TMS/SWD	I/O	JTAG mode select or SWD data
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
18	I/O	GPIO18	I/O	General-purpose input/output 18
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		PWMSYNCO	O	PWMSYNC output
		ECAP_APWMO	O	APWM mode output of the ECAP
		TCK/SWCK	I	JTAG clock or SWD clock
		Note: When TRSTn is high, the pin function is defined in Table 2-1.		
19	I/O	TRSTn	I	JTAG reset pin, reset the JTAG when low
20	1.2V Power	VCAP12	P	1.2 V power Add 2.2uF and 0.1uF bypass ceramic cap to GND

Pin	Type	Signal	Sub-Type ^[1]	Description
21	I/O	GPIO32	I/O	General-purpose input/output 32
		UART1_TXD	O	UART1 transmitted data
		I2C_SCL	I/O	I2C clock
		COMP_MON6	O	Comparator output monitor 6
22	I/O	GPIO33	I/O	General-purpose input/output 33
		UART1_RXD	I	UART1 received data
		I2C_SDA	I/O	I2C data
		COMP_MON7	O	Comparator output monitor 7
23	I/O	GPIO34	I/O	General-purpose input/output 34
		CAN_TXD	O	CAN transmitted data
		I2C_SCL	I/O	I2C clock
		EPWRTZ00	O	EPWRTZ0 output for monitoring
24	I/O	GPIO35	I/O	General-purpose input/output 35
		CAN_RXD	I	CAN received data
		I2C_SDA	I/O	I2C data
		EPWRTZ10	O	EPWRTZ1 output for monitoring
25	5V Power	DVDD5	P	5 V digital power Add 2.2uF and 0.1uF bypass ceramic cap to GND
26	5V Power	DVDD5EXT	P	5 V power for external loading Add 2.2uF bypass ceramic cap to GND
27	HV Power	VBAT	P	High voltage power from 5.5V to 42V Add 2.2uF and 0.1uF bypass ceramic cap to GND
28	HV Power	VBATM	P	High voltage power for vds monitor from 5.5V to 42V Add 0.1uF bypass ceramic cap to GND. Series 33 Ohm resistor from VBAT_D (VBAT for driver).
29	HV Power	VBATCP	P	High voltage power for charge-pump from 5.5V to 42V Add 2.2uF bypass ceramic cap to GND. Series 2 Ohm resistor from VBAT_D (VBAT for driver).
30	HV Power	VCP	P	Charge-pump output voltage, maximum up to 48V. Add 2.2uF ceramic cap to VBATCP.
31	HV Power	CFTOP0	P	Charge pump flying capacitor 0 top plate voltage Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0
32	HV Power	CFBOT0	P	Charge pump flying capacitor 0 bottom plate voltage

Pin	Type	Signal	Sub-Type ^[1]	Description
				Add 220nF ceramic cap as flying capacitor 0 between CFTOP0 and CFBOT0
33	HV Power	CFTOP1	P	Charge pump flying capacitor 1 top plate voltage Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1
34	HV Power	CFBOT1	P	Charge pump flying capacitor 1 bottom plate voltage Add 220nF ceramic cap as flying capacitor 1 between CFTOP1 and CFBOT1
35	HV IO	OUTL_W	O	Pre-Driver W-Phase low side FET gate drive
36	HV Power	VPX_W	P	Pre-Driver W-Phase power FET switching node
37	HV IO	OUTH_W	O	Pre-Driver W-Phase high side FET gate drive
38	HV IO	OUTL_V	O	Pre-Driver V-Phase low side FET gate drive
39	HV Power	VPX_V	P	Pre-Driver V-Phase power FET switching node
40	HV IO	OUTH_V	O	Pre-Driver V-Phase high side FET gate drive
41	HV IO	OUTL_U	O	Pre-Driver U-Phase low side FET gate drive
42	HV Power	VPX_U	P	Pre-Driver U-Phase power FET switching node
43	HV IO	OUTH_U	O	Pre-Driver U-Phase high side FET gate drive
44	Ground	VS_LOW	G	Pre-Driver low side ground
45	HV IO	MON	I	High voltage input for level monitor
46	HV IO	LIN	I/O	LIN bus interface, can be set as input or output.
47	HV Power	LIN_GND	P	LIN bus ground
48	5V I/O	XRSTn	I	Device reset pin, reset the device when low
49	3.3V Power	DVDD33	P	3.3 V digital power Add 4.7uF and 0.1uF bypass cap to GND
50	-2V ~ 3.3V input	PGAIN	AI	Differential PGA negative input
51	-2V ~ 3.3V input	PGAIP	AI	Differential PGA positive input
52	I/O	GPIO0	I/O	General-purpose input/output 0
		ANA_IN0	AI	Analog input channel 0
		PWMSOCAO	O	PWMSOCA output

Pin	Type	Signal	Sub-Type ^[1]	Description
		PWMSOCCO	O	PWMSOCC output
53	I/O	GPIO1	I/O	General-purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
		PWMSOCB	O	PWMSOCB output
		ECAP_APWMO	O	APWM mode output of the ECAP
54	I/O	GPIO2	I/O	General-purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
		DCLK	O	Clock output from CLKDET module for monitoring
		EPWRTZO	O	EPWRTZ output for monitoring It is the logic OR of EPWRTZ0O or EPWRTZ1O.
55	I/O	GPIO3	I/O	General-purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
		XIN	AI	External oscillator input
		COMP_MON0	O	Comparator output monitor 0
56	I/O	GPIO4	I/O	General-purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
		XOUT	O	External oscillator output
		COMP_MON1	O	Comparator output monitor 1
EPAD	Ground	GND	G	Exposed pad, connect to ground

[1] I = digital input, O = digital output or High-Voltage module output, AI = analog input, AO = analog output, P = power supply, G = ground.

[2] All GPIO pins can be configured as ECAP input.

3.3 GPIO pin function and state after reset

Table 3-3: GPIO pin function and state after reset

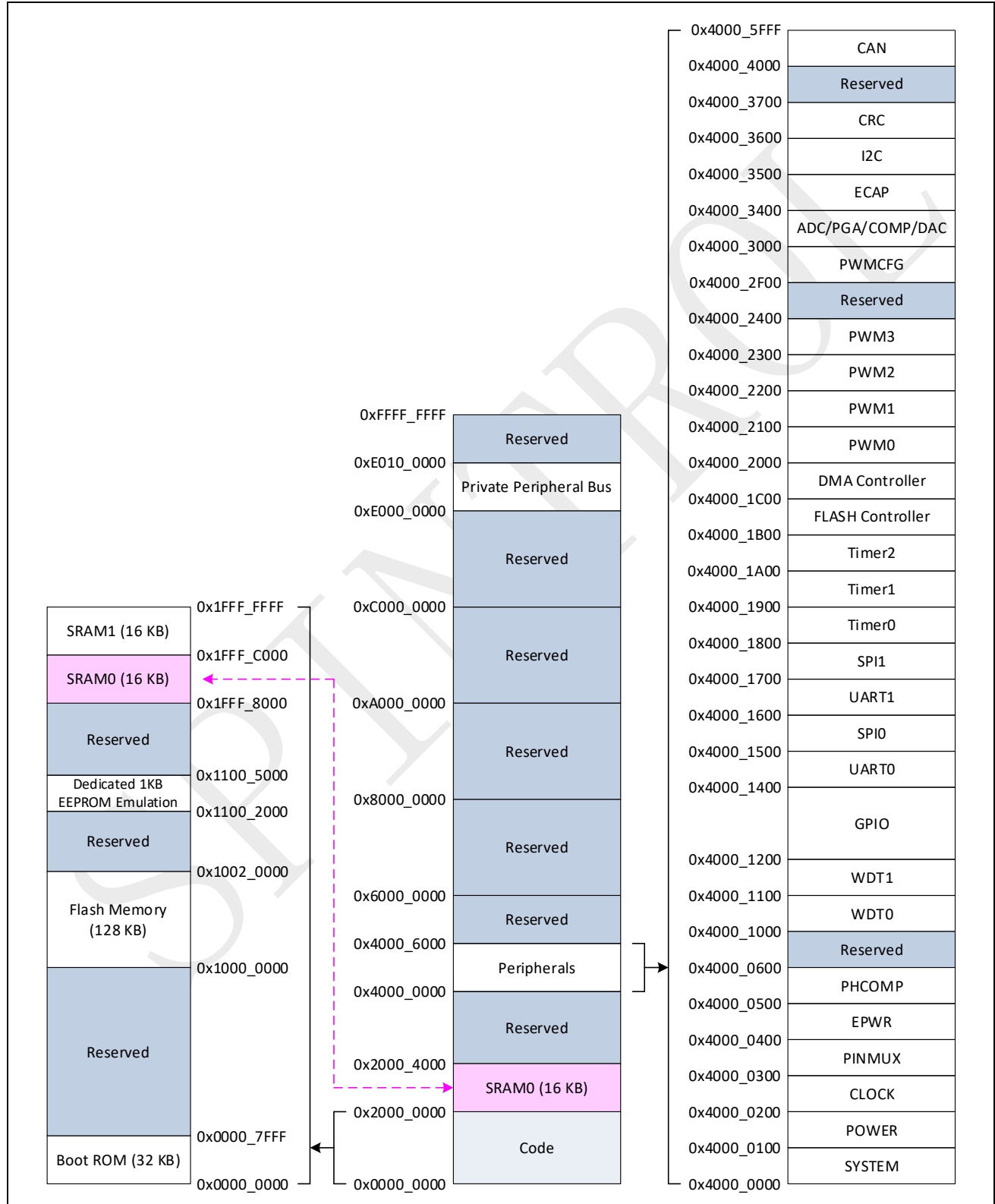
Pin Name	Default Function	Default State
GPIO0	ANA_IN0	Floating
GPIO1	ANA_IN1	Floating
GPIO2	ANA_IN2	Floating
GPIO3	ANA_IN3	Floating
GPIO4	ANA_IN4	Floating
GPIO5	GPIO5/BOOT	Pull down
GPIO6	GPIO6	Pull up
GPIO7	GPIO7	Pull up
GPIO8	GPIO8	Pull up
GPIO9	GPIO9	Pull up
GPIO10	GPIO10	Pull up
GPIO11	GPIO11	Pull up
GPIO12	GPIO12	Floating
GPIO13	GPIO13	Floating
GPIO14	GPIO14	Pull up
GPIO15	GPIO15	Pull up
GPIO16	GPIO16	Pull up
GPIO17	GPIO17	Pull up
GPIO18	GPIO18	Pull down
GPIO19	GPIO19	Floating
GPIO20	GPIO20	Floating
GPIO21	GPIO21	Floating
GPIO22	GPIO22	Floating
GPIO23	GPIO23	Floating
GPIO24	GPIO24	Floating
GPIO25	GPIO25	Pull up
GPIO26	GPIO26	Pull up
GPIO27	GPIO27	Pull down
GPIO28	ANA_IN5	Floating
GPIO29	ANA_IN6	Floating
GPIO30	ANA_IN7	Floating
GPIO31	ANA_IN8	Floating
GPIO32	GPIO32	Pull up
GPIO33	GPIO33	Pull up
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up

- [1] In SPD1177, GPIO19 ~ GPIO27 are internally connected to the High Voltage module as shown in [Figure 1-1](#), and not bonded out to the external pin. GPIO19 ~ GPIO24 are internally connected to the Pre-Driver module; GPIO25/GPIO26 are internally connected to LIN transceiver; GPIO27 is internally connected to the MON module.

4 Memory mapping

The memory map of SPD1177 is shown in [Figure 4-1](#).

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings^{[1][2]}

Symbol	Parameter	Min	Max	Unit
$V_{VBAT}^{[7]}$	Battery supply voltage for internal power system and LIN bus	-0.3	42	V
$V_{VBATM}^{[7]}$	Monitor pin for external supply of power MOS	-0.3	42	V
$V_{VBATCP}^{[7]}$	Battery supply voltage for internal charge-pump and pre-driver	-0.3	42	V
V_{LIN}	LIN bus interface, with respect to V_{LIN_GND}	-28	42	V
V_{MON}	High voltage input for level monitor	-28	42	V
V_{VCP}	Charge-pump voltage	-0.3	48	V
$V_{VCP} - V_{VBATCP}$	Charge-pump voltage minus battery supply voltage for internal charge-pump	-0.3	20	V
$V_{VPX_X}^{[4]}$	Pre-driver floating ground	-10	42	V
$V_{OUTH_X}^{[4]}$	Pre-driver high side output	-10	48	V
$V_{OUTH_X} \text{ vs } V_{PX_X}^{[4]}$	Pre-driver high side versus floating ground	-0.3	11 ^[5]	V
$V_{OUTL_X}^{[4]}$	Pre-driver low side output	-0.3	11 ^[5]	V
V_{VS_LOW}	Pre-driver low side ground	-2	2	V
V_{DVDD5}	DVDD5 voltage range for internal block	-0.3	7	V
$V_{DVDD5EXT}$	VDD5EXT voltage range for external circuit	-0.3	7	V
V_{DVDD33}	DVDD33 voltage range for internal MCU	-0.3	4.6	V
V_{VCAP12}	VCAP12 voltage range for internal MCU core	-0.3	1.5	V
V_{IN_3V}	3.3V IO input voltage	-0.3	$V_{DVDD33}+0.3$	V
$V_{LIN_GND}^{[6]}$	LIN bus ground.	-0.3	0.3	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature ^[3]	-40	+125	°C
T_{stg}	Storage temperature ^[3]	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to V_{GND} , unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

[4] X=U or V or W.

[5] Limited by design, internal circuit will turn on to clamp this voltage level.

[6] Short LIN_GND and GND on PCB board.

[7] Power ramp-up speed must be less than 1V/us, otherwise the device may be damaged permanently.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
V_{VBAT}	Battery supply voltage for internal power system and LIN bus	—	5.5	—	28	V
	Extend range ^[1] for V_{VBAT}	—	28	—	40	V
	Supply voltage with reduced functionality (Micro controller/Flash with full operation)	—	4.5	—	5.5	V
V_{VBATM}	Battery supply voltage for internal pre-driver	—	5.5	—	28	V
	Extend range ^[1] for V_{VBATM}	—	28	—	40	V
V_{VBATCP}	Battery supply voltage for internal charge-pump	—	5.5	—	28	V
	Extend range ^[1] for V_{VBATCP}	—	28	—	40	V
V_{DVDD5}	DVDD5 voltage range for internal block	—	4.5	5.0	5.5	V
$V_{DVDD5EXT}$	VDD5EXT voltage range for external loading	—	4.5	5.0	5.5	V
V_{DVDD33}	DVDD33 voltage range for internal MCU	—	2.97	3.3	3.63	V
V_{VCAP12}	VCAP12 voltage range for internal MCU core	—	1.08	1.2	1.32	V
V_{GND}	Supply ground	—	—	0	—	V
V_{IH_DIG}	Digital I/O high-level input voltage	—	—	2.4	—	V
V_{IL_DIG}	Digital I/O low-level input voltage	—	—	0.8	—	V
I_{OH_DIG}	3.3V high-level output source current when $V_{OH} = 2.1V$, $V_{DVDD5} = 2.6V$	STRENGTH=0 STRENGTH=1	—	-0.23 -4.1	TBD TBD	mA
I_{OL_DIG}	3.3V low-level output sink current when $V_{OL} = 0.5V$, $V_{DVDD5} = 2.6V$	STRENGTH=0 STRENGTH=1	—	-0.97 -14.5	TBD TBD	mA
V_{IH_3V}	3.3V high-level input voltage	$V_{DVDD33} = 3.3V$	2.0	—	$V_{DVDD33} + 0.3$	V
V_{IL_3V}	3.3V low-level input voltage	$V_{DVDD33} = 3.3V$	$V_{GND} - 0.3$	—	0.8	V
I_{OH_3V}	3.3V high-level output source current when $V_{OH} = V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	—	—	4.5 9 13.5 18	mA
I_{OL_3V}	3.3V low-level output sink current when $V_{OL} = V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2	—	—	4.5 9 13.5	mA

Symbol	Parameter	Conditions	Min	Nom	Max	Unit
		STRENGTH=3			18	
T _J	Junction temperature		-40	—	+125	°C

- [1] This extend voltage range is only allowed for a short duration: $t_{max} \leq 400$ ms and with parameter deviation for function. Continuous operation at this extend voltage range is not allowed. This feature is not specifically stated in the subsequent tables, and it has this meaning.

5.3 I/O Electrical characteristics

Table 5-3: 3.3V IO Electrical characteristics ($V_{DVDD33} = 3.3V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	$I_{OH} = I_{OHMAX}$	$V_{DVDD33} - 0.66$	—	—	V
V_{OL}	Low-level output voltage	$I_{OL} = I_{OLMAX}$	—	—	0.66	V
V_{IH}	High-level input voltage	—	2.0	—	$V_{DVDD33} + 0.3$	V
V_{IL}	Low-level input voltage	—	$V_{GND} - 0.3$	—	0.8	V
I_{OH}	High-level output source current when $V_{OH} = V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	—	—	4.5 9 13.5 18	mA
I_{OL}	Low-level output sink current when $V_{OL} = V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	—	—	4.5 9 13.5 18	mA
I_{IL}	Low-level input current (Pin with pull-up and pull-down both disabled)	$V_{DVDD33} = 3.3V$ $V_{IH} = 0V$	—	—	10	uA
I_{IH}	High-level input current (Pin with pull-up and pull-down both disabled)	$V_{DVDD33} = 3.3V$ $V_{IH} = V_{DVDD33}$	—	—	10	uA
R_{PU}	Input pull-up resistor	$V_{IO} = 0V$	—	41	—	kΩ
R_{PD}	Input pull-down resistor	$V_{IO} = V_{DVDD33}$	—	42	—	kΩ

5.4 Power mode transition time

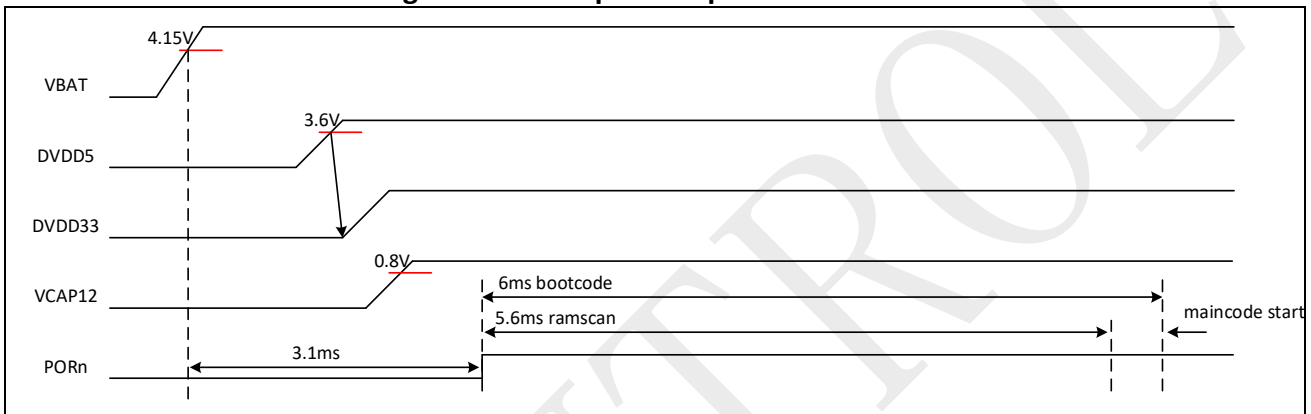
Table 5-4: Power mode transition time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{stop,entry}$	Stop mode entry time	—	—	25	—	us
$t_{stop,exit}$	Stop mode exit time (to user's code)	—	—	1	—	ms
$t_{sleep,entry}$	Sleep mode entry time	—	—	25	—	us
$t_{sleep,exit}^{[1]}$	Sleep mode exit time (to user's code)	—	—	7.4	—	ms
$t_{power-up}^{[2]}$	Cold power-up time (to user's code)	—	—	9.1	—	ms

[1] It contain ~5.63ms for the RAM self-test.

[2] Compared with sleep mode exit time, it contain extra ~1.7ms POR time for VBAT.

Figure 5-1: Cold power-up transition time



5.5 Power consumption

Typical current consumption

In active mode, the SPD1177 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is 1), except DGCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.
- Charge pump enable, Pre-driver toggle and no external driver MOS.
- GPIO5 is connected to GND

In stop mode, the SPD1177 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO, ROSC and XO) are disabled;
- 5V/3.3V/1.2V LDOs are in low power mode;
- GPIO5 is connected to GND

In sleep mode, the SPD1177 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are disabled;
- Clock modules (PLL, RCO, ROSC and XO) are disabled;
- 5V/3.3V/1.2V LDOs are shut down to 0V;
- GPIO5 is connected to GND

The typical operational current consumption over various HCLK frequency is shown in Figure 5-2.

Figure 5-2: Typical operational current versus frequency

TBD

Table 5-5: SPD1177 current consumption ($V_{BAT} = 18V$) (TBD)

Conditions	Junction Temperature T_J (°C)						Unit
	25	85	105	125	150	175	
Active mode ($f_{HCLK} = f_{PLL} = 100$ MHz)	TBD	TBD	TBD	TBD	TBD	TBD	mA
Active mode ($f_{HCLK} = f_{PLL} = 32$ MHz)	TBD	TBD	TBD	TBD	TBD	TBD	mA
Stop mode ^[1]	TBD	TBD	TBD	TBD	TBD	TBD	mA
Sleep mode	TBD	TBD	TBD	TBD	TBD	TBD	mA

[1] Stop mode support T_J from -40 °C to 105 °C.

Table 5-6: SPD1177 active current consumption ($V_{BAT} = 28V$) (TBD)

Conditions	Junction Temperature T_J (°C)						Unit
	25	85	105	125	150	175	
Active mode ($f_{HCLK} = f_{PLL} = 100$ MHz)	TBD	TBD	TBD	TBD	TBD	TBD	mA
Active mode ($f_{HCLK} = f_{PLL} = 32$ MHz)	TBD	TBD	TBD	TBD	TBD	TBD	mA
Stop mode ^[1]	TBD	TBD	TBD	TBD	TBD	TBD	mA
Sleep mode	TBD	TBD	TBD	TBD	TBD	TBD	mA

[1] Stop mode support T_J from -40 °C to 105 °C.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-7. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
 - With all peripherals clocked disabled
 - With only one peripheral enabled

Table 5-7: Peripheral current consumption

Peripherals ^[1]	Conditions	Typ ^[2]	Unit
BOD	Select RCO as system clock source; All other peripherals are in default settings	106.0	uA
ADC ^[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; $f_{HCLK} = 100\text{ MHz}$, $f_{PLL} = 100\text{ MHz}$	8854.0	uA
Monitoring ADC ^[3]		2989.0	uA
T-Sensor		157.0	uA
DPGA ^[4]		1106.0	uA
SPGA ^[4]		156.0	uA
DAC buffer		274.0	uA
DAC		327.0	uA
Phase Comparator		126.0	uA
Comparator		105.0	uA
UART	UART clock 100MHz, 512000 bps	383.0	uA
SPI	SPI clock 100MHz, 20Mbps	284.0	uA
I2C	I2C clock 100MHz, 100Kbps	436.0	uA
CAN	CAN clock 100MHz, 1Mbps + 8Mbps	3526.0	uA
PWM (Without Pre-Driver)	PWM clock 100MHz and toggle frequency 15kHz	302.5	uA
PWM (With Pre-Driver)	PWM clock 100MHz, PWM toggle frequency 15kHz	TBD	uA
ECAP	ECAP clock 100MHz	324.0	uA
WDT	WDT clock 100MHz	220.0	uA
TIMER	TIMER clock 100MHz	144.0	uA
FLASH	HCLK clock 100MHz	306.0	uA
XO	HCLK is from 100MHz PLL, which takes RCO as input	736.0	uA
RCO	HCLK is from 100MHz PLL, which takes XO (32MHz) as input	254.0	uA
PLL	XO (32MHz) as HCLK source, $f_{PLL} = 100\text{ MHz}$	961.0	uA
LIN transceiver	UART clock 100MHz, 19200bps	TBD	uA
DVDD5EXT	–	42.4	uA

[1] For peripherals with multiple instances, the current quoted is for single modules (result of average).

[2] Typical values are measured at $T_A = 25\text{ }^{\circ}\text{C}$, $V_{BAT} = 12\text{ V}$.

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.6 BOD characteristics

Table 5-8: VCAP12 BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(VCAP12OV)$	VCAP12 over-voltage assert threshold	—	—	1.36	—	V
$V_{th0}(VCAP12OV)$	VCAP12 over-voltage release threshold	—	—	1.33	—	V
$V_{th1}(VCAP12UV)$	VCAP12 under-voltage assert threshold	—	—	1.07	—	V
$V_{th0}(VCAP12UV)$	VCAP12 under-voltage release threshold	—	—	1.10	—	V

Table 5-9: DVDD33 BOD^[1] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(DVDD33OV)$	DVDD33 over-voltage assert threshold	—	—	3.66	—	V
$V_{th0}(DVDD33OV)$	DVDD33 over-voltage release threshold	—	—	3.53	—	V
$V_{th1}(DVDD33UV)$	DVDD33 under-voltage assert threshold	—	—	2.94	—	V
$V_{th0}(DVDD33UV)$	DVDD33 under-voltage release threshold	—	—	3.03	—	V

[1] Brown-out detector for DVDD33 in MCU.

Table 5-10: DVDD33 BOD1^[1] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(DVDD33OV)$	DVDD33 over-voltage assert threshold	—	—	3.64	—	V
$V_{th0}(DVDD33OV)$	DVDD33 over-voltage release threshold	—	—	3.52	—	V
$V_{th1}(DVDD33UV)$	DVDD33 under-voltage assert threshold	—	—	2.57	—	V
$V_{th0}(DVDD33UV)$	DVDD33 under-voltage release threshold	—	—	3.70	—	V

[1] Brown-out detector for DVDD33 in high voltage.

Table 5-11: VBAT BOD^[1] characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(VBATOV)$	VBAT over-voltage assert threshold	—	—	44.0	—	V
$V_{th0}(VBATOV)$	VBAT over-voltage release threshold	—	—	38.3	—	V
$V_{th1}(VBATUV)$	VBAT under-voltage assert threshold	—	—	5.00	—	V
$V_{th0}(VBATUV)$	VBAT under-voltage release threshold	—	—	5.20	—	V

[1] VBATCP use the same threshold setting from VBAT.

Table 5-12: DVDD5 BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(DVDD5OV)$	DVDD5 over-voltage assert threshold	—	—	5.68	—	V
$V_{th0}(DVDD5OV)$	DVDD5 over-voltage release threshold	—	—	5.60	—	V
$V_{th1}(DVDD5UV)$	DVDD5 under-voltage assert threshold	—	—	4.40	—	V
$V_{th0}(DVDD5UV)$	DVDD5 under-voltage release threshold	—	—	4.50	—	V

Table 5-13: DVDD5EXT BOD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1}(DVDD5EXTOV)$	DVDD5EXT over-voltage assert threshold	—	—	5.68	—	V
$V_{th0}(DVDD5EXTOV)$	DVDD5EXT over-voltage release threshold	—	—	5.60	—	V
$V_{th1}(DVDD5EXTUV)$	DVDD5EXT under-voltage assert threshold	—	—	4.40	—	V
$V_{th0}(DVDD5EXTUV)$	DVDD5EXT under-voltage release threshold	—	—	4.50	—	V

Table 5-14: (VCP – VBATCP) BOD characteristics

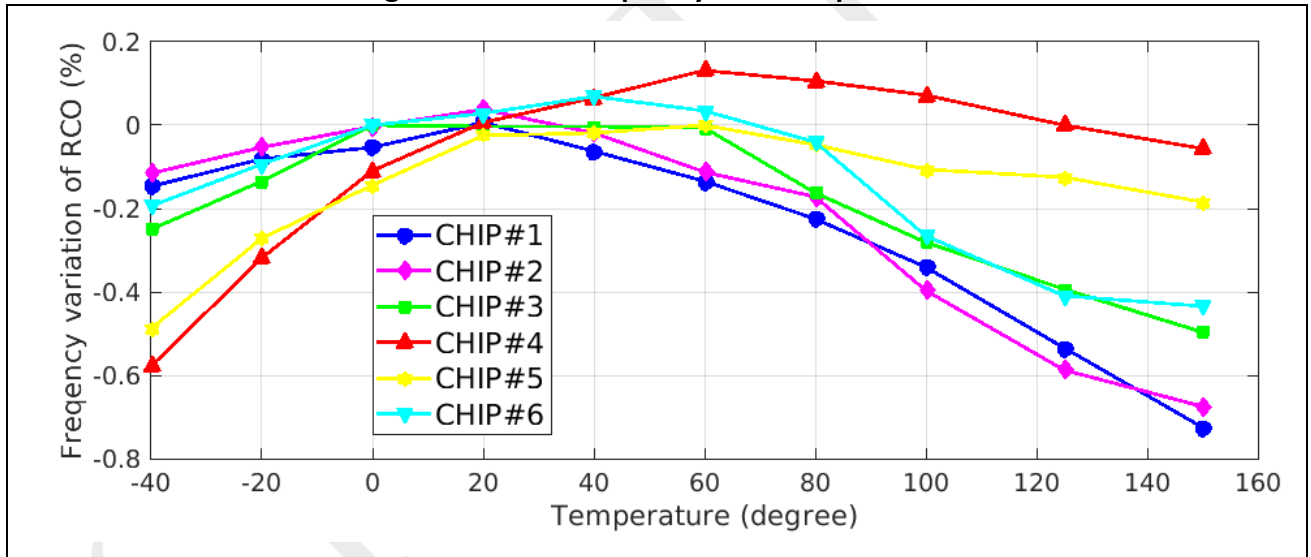
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1((VCP-VBATCP)OV)}$	(VCP – VBATCP) over-voltage assert threshold	–	–	14.81	–	V
$V_{th0((VCP-VBATCP)OV)}$	(VCP – VBATCP) over-voltage release threshold	–	–	14.57	–	V
$V_{th1((VCP-VBATCP)UV)}$	(VCP – VBATCP) under-voltage assert threshold	–	–	6.097	–	V
$V_{th0((VCP-VBATCP)UV)}$	(VCP – VBATCP) under-voltage release threshold	–	–	6.206	–	V

5.7 RCO characteristics

Table 5-15: RCO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{RCO}	RCO frequency	$T_J = 25\text{ }^{\circ}\text{C}$	–	32	–	MHz
E_{RCO}	f_{RCO} error (RCO frequency variation versus temperature)	$T_J = -40\sim 150\text{ }^{\circ}\text{C}$	-1.5	–	1.5	%
t_{settle}	RCO frequency ready time	$E_{RCO} < 1\%$	–	4.2	–	us

Figure 5-3: RCO frequency with temperature



5.8 PLL characteristics

Table 5-16: PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{VCO}	VCO frequency	$T_J = -40\sim 150\text{ }^{\circ}\text{C}$	400	500	600	MHz
$f_{PFD}^{[1]}$	Phase-Frequency Detector (PFD) input frequency	–	4	–	8	MHz
$t_{lock}^{[1]}$	Locking time	$T_J = 25\text{ }^{\circ}\text{C}$	–	10	15	us
t_{jitter}	PLL output clock jitter	$T_J = 25\text{ }^{\circ}\text{C}$	–	40	–	ps

[1] Not subject to production test, guaranteed by design.

5.9 XO characteristics

Table 5-17: XO characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{XO}	XO frequency	$T_J = -40 \sim 150\text{ }^{\circ}\text{C}$	4	–	32	MHz

5.10 ROSC characteristics

Table 5-18: ROSC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ROSC}	ROSC frequency	$T_J = -40 \sim 150\text{ }^{\circ}\text{C}$	16	32	48	MHz

5.11 13-bit ADC characteristics

Table 5-19: ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_R	Resolution	No missing code. Monotonic	13	–	–	bits
f_S	Conversion speed ^[1]	–	–	–	2.5	MSPS
V_{in}	Input voltage range	–	0	–	V_{DDA}	V
V_{ref}	Reference voltage	–	1.194	1.2	1.206	V
I_{on}	Operational current	$V_{DVDD33} = 3.3\text{ V}$	–	8.5	11.5	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.5	LSB
E_{offset}	Offset error ^[2]	With calibration	-4	± 2	4	LSB
E_{gain}	Gain error ^[2]	With calibration	-40	± 4	40	LSB
T_{coef}	ADC temperature coefficient with internal reference	–	–	30	–	ppm/ $^{\circ}\text{C}$
t_{settle} ^[3]	Power-up time	–	–	–	100	us
$ENOB_{DC}$	DC Noise Floor	–	–	11.5	–	bits
SNR	Signal-to-noise ratio	$f_{in} = 100\text{ kHz},$ $V_{in} = 0.94FS,$ $N = 8192$	–	71	–	dBFS
THD	Total harmonic distortion		–	-84	–	dBFS
ENOB	Effective number of bits		–	11.4	–	bits
SFDR	Spurious free dynamic range		–	80	–	dBFS

[1] Sampling time = 200ns, conversion time = 200ns.

[2] Offset and gain can be calibrated automatically by hardware.

[3] Not subject to production test, guaranteed by design.

5.12 Monitoring ADC characteristics

Table 5-20: Monitoring ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_R	Resolution	No missing code. Monotonic	13	–	–	bits
f_s	Conversion speed ^[1]	–	–	–	500	KSPS
V_{in}	Input voltage range	–	0	–	V_{DVDD33}	V
V_{ref}	Reference voltage	–	1.19	1.2	1.21	V
I_{on}	Operational current	$V_{DVDD33} = 3.3\text{ V}$	–	2.8	3.6	mA
INL	Integral linearity error	–	-3.0	-	3.0	LSB
DNL	Differential linearity	–	-1.0	-	1.0	LSB
E_{offset}	Offset error	With calibration	-4	± 2	4	LSB
E_{gain}	Gain error	With calibration	-40	± 4	40	LSB
$ENOB_{DC}$	DC Noise Floor	–	–	11.5	–	bits
SNR	Signal-to-noise ratio	$f_{in} = 50\text{kHz}$, $V_{in} = 0.94FS$, $N = 4096$	–	71	–	dBFS
THD	Total harmonic distortion		–	-84	–	dBFS
ENOB	Effective number of bits		–	11.4	–	bits
SFDR	Spurious free dynamic range		–	80	–	dBFS

[1] Sampling time = 1 μ s, conversion time = 1 μ s.

5.13 Temperature sensor characteristics

Table 5-21: Temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$TMCU_{slope}$	When the temperature sensor is measured by the ADC, for each increase of 1 LSB in the ADC output code, the corresponding temperature value changes.	–	–	3.7	–	°C/LSB
$TPMU_{slope}$		–	–	-0.48	–	°C/LSB
$TLIN_{slope}$		–	–	-0.48	–	°C/LSB
$TMCU_{offset}$	The code obtained by ADC measuring the temperature sensor.	$T_J = 25\text{ °C}$	–	-81	–	LSB
$TPMU_{offset}$			–	-772.8	–	LSB
$TLIN_{offset}$			–	-772.8	–	LSB

5.14 DPGA characteristics

Table 5-22: DPGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Differential input range	—	-2.7/G	—	+2.7/G	V
V_{out}	Output voltage range	—	0.3	—	$V_{D33}-0.3$	V
R_{in}	Input impedance	—	—	4	—	k Ω
G	Gain	Differential	2, 4, 8, 16, 24, 32, 48, 64			-
E_{gain}	Gain error	Differential Gain = 2	-1.5	—	1.5	%
		Differential Gain = 16	-1	—	1	%
		Differential Gain = 64	-1	—	1	%
V_{offset}	Offset	Differential Gain=2	-3	—	9	mV
		Differential Gain=16	-2	—	4	mV
		Differential Gain=64	-2	—	4	mV
V_{CM}	Common mode input voltage range	Differential gain = 2	-1.34	—	2	V
		Differential gain = 4	-0.8	—	2	V
		Differential gain = 8	-0.4	—	2	V
		Differential gain = 16	-0.2	—	2	V
		Differential gain = 24	-0.19	—	2	V
		Differential gain = 32	-0.15	—	2	V
		Differential gain = 48	-0.1	—	2	V
		Differential gain = 64	-0.08	—	2	V
t_{settle}	Settle time ^[1]	Differential gain = 2	—	313.7	441.6	ns
		Differential gain = 4	—	303.1	425.5	ns
		Differential gain = 8	—	268.4	423.8	ns
		Differential gain = 16	—	376.7	604.7	ns
		Differential gain = 24	—	355.8	598.9	ns
		Differential gain = 32	—	442.9	742.3	ns
		Differential gain = 48	—	628.0	1061.0	ns
		Differential gain = 64	—	813.3	1378.0	ns
GBW	Gain bandwidth ^[2]	Differential gain = 2	6	9.68	—	MHz
		Differential gain = 4	3.8	6.07	—	MHz
		Differential gain = 8	2.56	3.45	—	MHz
		Differential gain = 16	1.37	1.85	—	MHz
		Differential gain = 24	1.23	1.63	—	MHz
		Differential gain = 32	0.93	1.23	—	MHz
		Differential gain = 48	0.63	0.83	—	MHz
		Differential gain = 64	0.4	0.63	—	MHz
SR	Slew rate ^[3]	Differential gain = 2	15	21	30	V/ μ s
		Differential gain = 4	15	21	30	V/ μ s
		Differential gain = 8	14.5	21	30	V/ μ s
		Differential gain = 16	11.2	18.9	29.7	V/ μ s
		Differential gain = 24	12.57	21	33.4	V/ μ s
		Differential gain = 32	9.25	18.4	31.8	V/ μ s
		Differential gain = 48	6.1	11.5	25	V/ μ s
		Differential gain = 64	4.6	8.6	17.6	V/ μ s

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ENOB _{DC}	Effective number of bits	Differential Gain = 2	—	11.93	—	bits
		Differential Gain = 16	—	11.57	—	bits
		Differential Gain = 64	—	10.94	—	bits
SNR	Signal-to-noise ratio at 10kHz input	Differential Gain = 2	—	72.2	—	dBFS
		Differential Gain = 16	—	71.1	—	dBFS
		Differential Gain = 64	—	64.8	—	dBFS
THD	Total harmonic distortion at 10kHz input	Differential Gain = 2	—	79.59	—	dBFS
		Differential Gain = 16	—	81.29	—	dBFS
		Differential Gain = 64	—	78.47	—	dBFS
CMRR _{DC}	DC common mode rejection Ratio	Differential Gain = 2	—	-59.7	—	dBFS
		Differential Gain = 16	—	-52.6	—	dBFS
		Differential Gain = 64	—	-61	—	dBFS
PSRR _{DC}	Power Supply Rejection Ratio	Differential Gain = 2	—	-72.8	—	dBFS
		Differential Gain = 16	—	-84.9	—	dBFS
		Differential Gain = 64	—	-93.4	—	dBFS
I _{on}	Current consumption	Differential Gain=2	—	1.215	—	mA
		Differential Gain=16	—	1.096	—	mA
		Differential Gain=64	—	1.152	—	mA

- [1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V ($V_{DD33}=3.3V$), the time for output to be settled to 98%, guarantee by design.
- [2] GBW data is guaranteed by design.
- [3] Slew rate data is from 10% to 90% of output signal, guaranteed by design.

Figure 5-4: Settling time with different gain

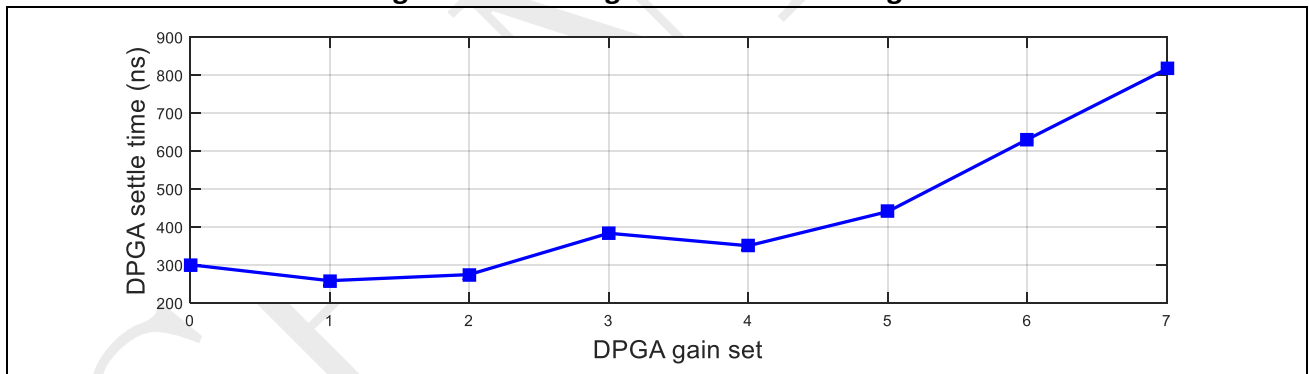


Figure 5-5: ENOB_DC with different gain

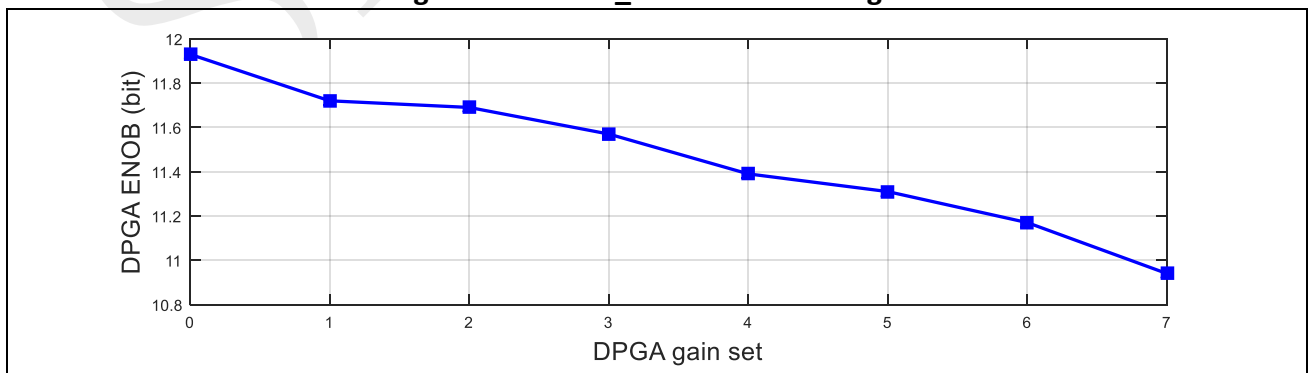
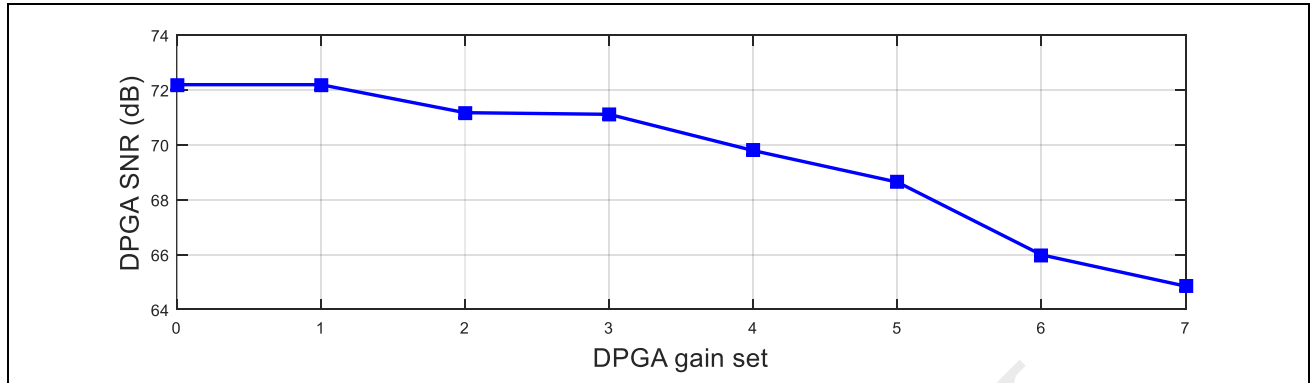
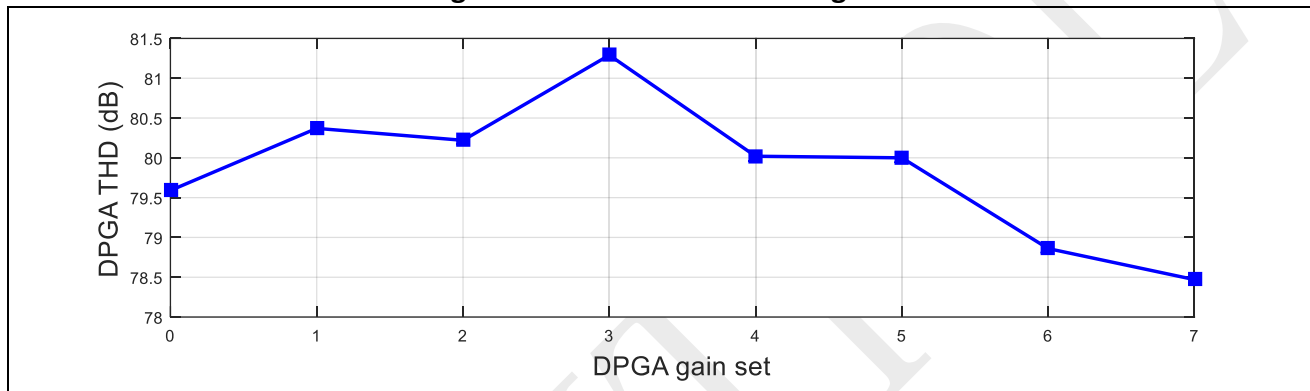
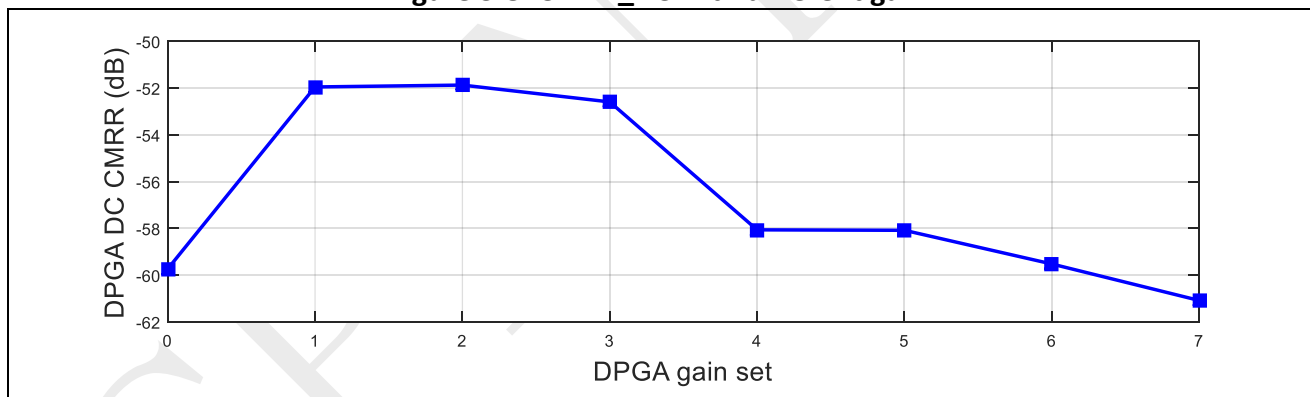
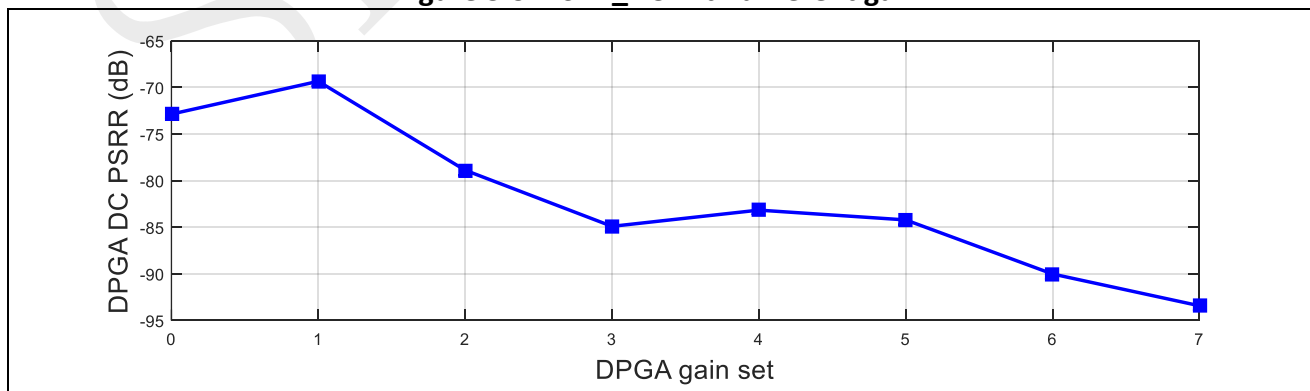


Figure 5-6: SNR with different gain**Figure 5-7: THD with different gain****Figure 5-8: CMRR_DC with different gain****Figure 5-9: PSRR_DC with different gain**

5.15 SPGA characteristics

Table 5-23: SPGA characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input range	—	0.3	—	$V_{DDA}-1.3$	V
V_{out}	Output voltage range	—	0.3	—	$V_{DDA}-0.3$	V
R_{in}	Input impedance	—	—	High-Z	—	Ω
G	Gain	Single-ended	1, 2, 4, 8, 16, 32, 48, 64			-
E_{gain}	Gain error	Gain = 2	-1	—	1	%
		Gain = 32	-1.2	—	1.2	%
		Gain = 64	-2	—	2	%
V_{offset}	Offset	—	-10	—	5	mV
t_{settle}	Settle time	Gain = 2	—	300	—	ns
		Gain = 32	—	1000	—	ns
		Gain = 64	—	2000	—	ns
ENOB	Effective number of bits	Gain = 2	—	11	—	bits
		Gain = 32	—	9	—	bits
		Gain = 64	—	8	—	bits
I_{on}	Current consumption	—	—	0.5	—	mA

Figure 5-10: Settling time with different gain

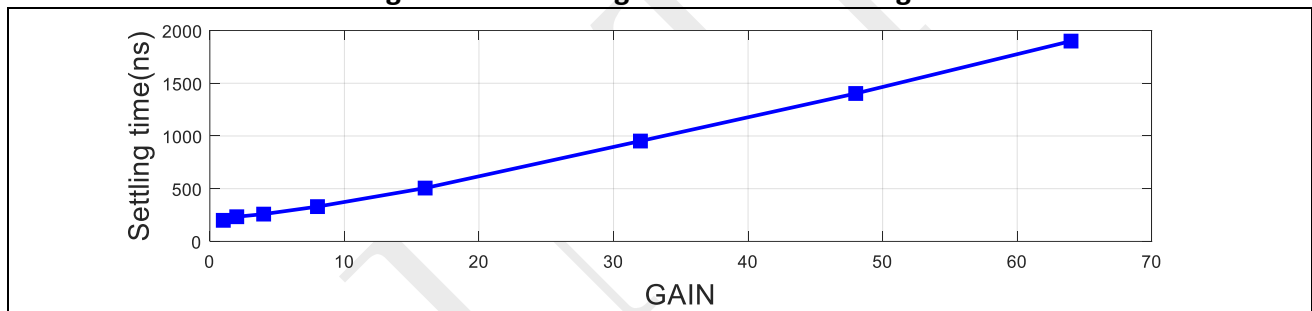
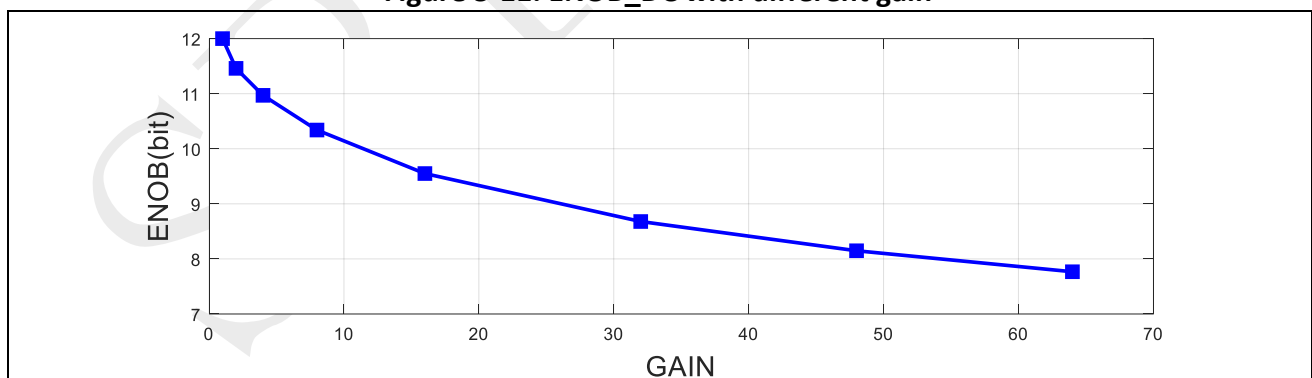


Figure 5-11: ENOB_DC with different gain



5.16 Analog comparator characteristics

Table 5-24: Analog comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage range	-	0	—	V_{DVDD33}	V
V_{offset}	Offset voltage (Hysteresis voltage option = 0)	$V_{DVDD33} = 3.3V$, $T_J = 25^{\circ}C$, $V_{cm} = 1.65V$	-10	—	10	mV
V_{hyst}	Hysteresis voltage option = 0		—	0	—	mV
	Hysteresis voltage option = 1		—	13	—	mV
	Hysteresis voltage option = 2		—	25	—	mV
	Hysteresis voltage option = 3		—	37	—	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		—	50	—	ns

5.17 Phase comparator characteristics

Table 5-25: Phase comparator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Input voltage range	—	0	—	V_{DVDD33}	V
V_{offset}	Offset voltage (Hysteresis voltage=0)	$V_{DVDD33} = 3.3V$, $T_J = 25^{\circ}C$, $V_{cm} = 1.65V$	-3.5	—	3.5	mV
V_{hyst}	Hysteresis voltage option = 0		—	0	—	mV
	Hysteresis voltage option = 1		—	13	—	mV
	Hysteresis voltage option = 2		—	25	—	mV
	Hysteresis voltage option = 3		—	37	—	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		—	250	—	ns

5.18 Internal 10-bit DAC characteristics

Table 5-26: DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N	Resolution	Monotonic	10	—	—	bit
V_{FS}	Full scale value	—	0	—	$V_{D VDD33}$	V
DNL	Differential linearity	—	-0.5	—	0.5	LSB
INL	Integral linearity	—	-1	—	1	LSB
E_{offset}	Offset error	—	—	5	—	mV
$t_{settle}^{[1]}$	DAC settling time	—	—	—	1	us

[1] Guaranteed by design.

Figure 5-12: DNL curve

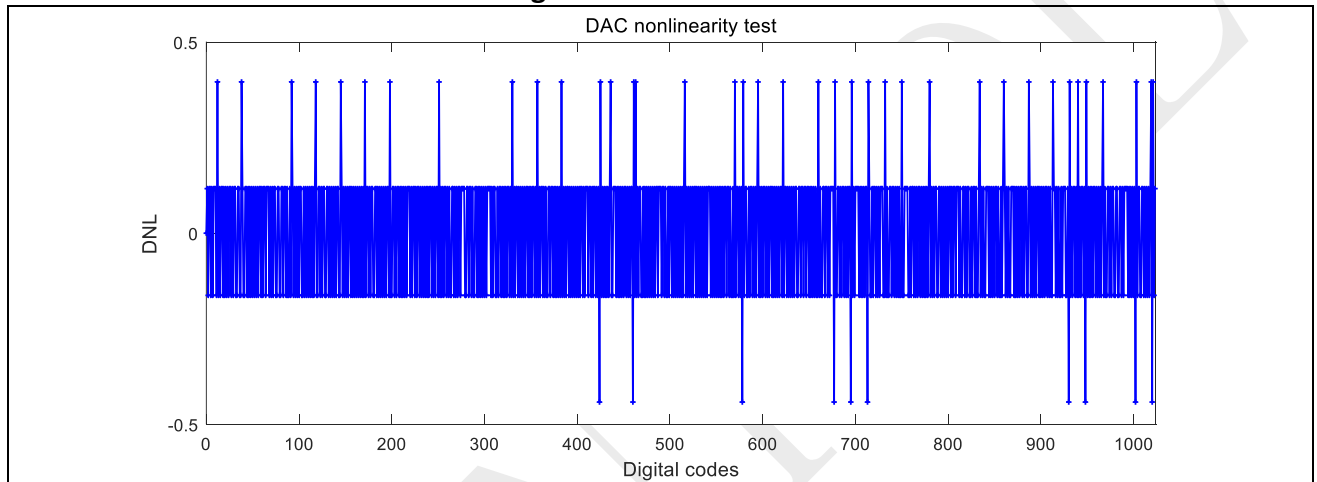
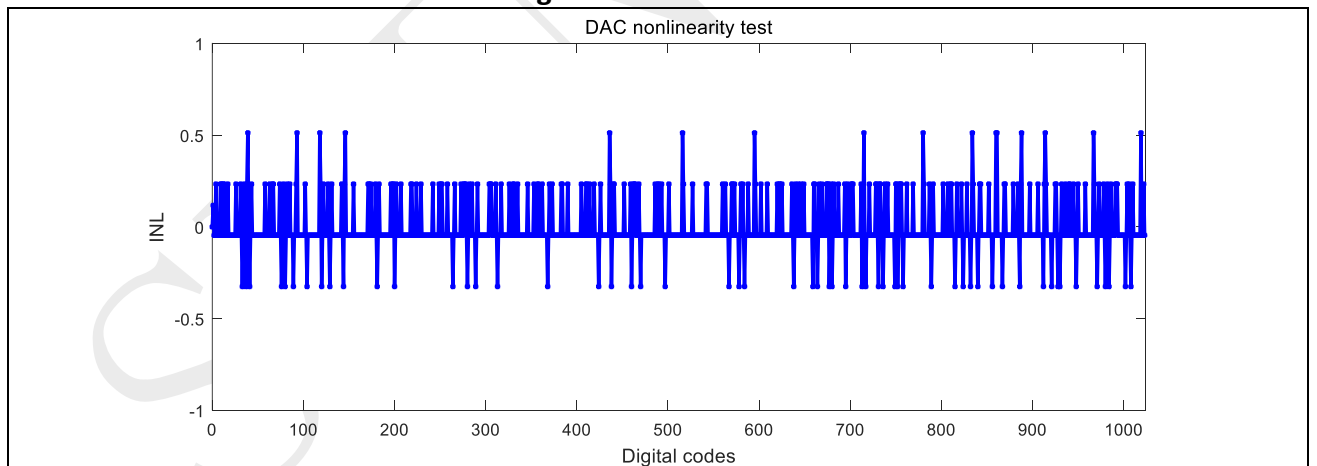


Figure 5-13: INL curve



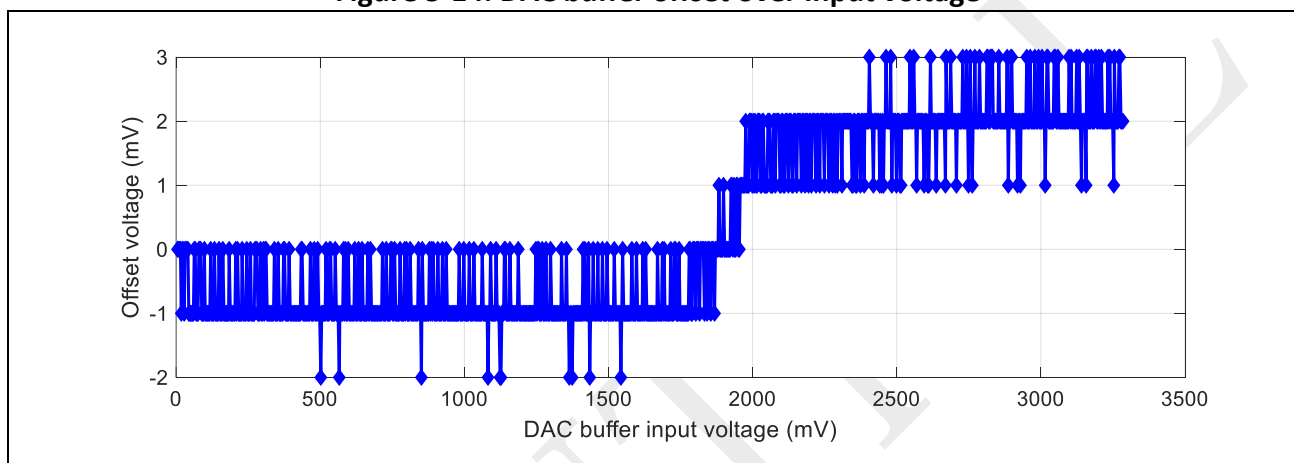
5.19 DAC buffer characteristics

Table 5-27: DAC buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{out}	Output voltage range	—	0.3	—	$V_{DD33}-0.4$	V
$t_{settle}^{[1]}$	Settling time	—	—	1	—	us
E_{offset}	Offset error	—	—	5	—	mV
$C_L^{[1]}$	Capacitor load	—	—	—	50	pF
$R_L^{[1]}$	Resistor load	—	5K	—	—	Ω

[1] Not subject to production test, guaranteed by design.

Figure 5-14: DAC buffer offset over Input voltage



5.20 D2S buffer characteristics

Table 5-28: D2S buffer characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{out}	Output voltage range	—	0.3	—	$V_{DD33}-0.3$	V
t_{settle}	Settling time ^[1]	—	—	10	—	ms
E_{offset}	Offset error	—	—	10	—	mV
E_{gain}	Gain error	—	—	1	—	%
C_L	Capacitor load	—	—	1	—	uF
I_{on}	Current consumption	—	—	1	—	mA

[1] Settling time is measured by adding external RC filter, typical value is $R=1k\Omega$, $C=1\mu F$.

5.21 Pre-Driver characteristics

Table 5-29: Pre-Driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBATM} ,	Input supply voltage	–	5.5	–	28	V
V_{VBATCP}	Extend supply range	–	28	–	40	V
OUTH-VPX	Pre-driver high side versus floating ground	VPX=VBAT Max driving capability	6.75 ^[1]	9.4 ^[1]	–	V
		VPX=0 Max driving capability	10 ^[1]	10 ^[1]	–	V
OUTL-GND	Pre-driver low side output, with respect to V_{GND}	VPX=VBAT Max driving capability	10 ^[1]	10 ^[1]	–	V
		VPX=0 Max driving capability	10 ^[1]	10 ^[1]	–	V
D_{MAX}	Maximum supported duty cycle	–	–	100	–	%
$t_{DL,MINC}$	Low-side propagation delay, min current strength code	1nF Capacitor as load	–	1150	–	ns
$t_{DH,MINC}$	High-side propagation delay, min current strength code	1nF Capacitor as load	–	1150	–	ns
$t_{DL,MAXC}$	Low-side propagation delay, max current strength code	1nF Capacitor as load	–	170	–	ns
$t_{DH,MAXC}$	High-side propagation delay, max current strength code	1nF Capacitor as load	–	170	–	ns
Δt	High/Low side delay mismatch	–	–	30	TBD	ns
$t_{r,MINC}$	Rise time, min code	1nF Capacitor as load	–	1100	–	ns
$t_{f,MINC}$	Fall time, min code	1nF Capacitor as load	–	900	–	ns
$t_{r,MAXC}$	Rise time, max code	1nF Capacitor as load	–	52	–	ns
$t_{f,MAXC}$	Fall time, max code	1nF Capacitor as load	–	48	–	ns
VPX_{MIN}	High side return ground Minimum	Min voltage where high side signal still propagates	-10	–	–	V
V_{th,ds_mon}	Threshold for drain vs source voltage monitor	Threshold option = 1	0.24	0.3	0.36	V
$I_{Source_Max_HS}$	Source current - Charge current - High Side Driver	$V_{VBATM} = V_{VBATCP} = 8V$ maximum strength	TBD	300	TBD	mA
$I_{Sink_Max_HS}$	Sink current - Discharge current-High Side Driver		TBD	300	TBD	mA
$I_{Source_Max_LS}$	Source current - Charge current - Low Side Driver		TBD	300	TBD	mA
$I_{Sink_Max_LS}$	Sink current - Discharge current-Low Side Driver		TBD	300	TBD	mA

[1] Minimum value when $V_{VBATM} = V_{VBATCP} = 5.5V$. Typical value when $V_{VBATM} = V_{VBATCP} = 12V$.

Figure 5-15: Pre-Driver maximum sourcing/sinking current measurement (low side)

TBD

- [1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 100mA/div).
 [2] Pre-driver output charging 47nF capacitor.

Figure 5-16: Pre-Driver maximum sourcing/sinking current measurement (high side)

TBD

- [1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 100mA/div).
 [2] Pre-driver output discharging 47nF capacitor.

Figure 5-17: Pre-Driver minimum sourcing/sinking current measurement (low side)

TBD

- [1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 10mA/div).
 [2] Pre-driver output discharging 10nF capacitor.

Figure 5-18: Pre-Driver minimum sourcing/sinking current measurement (high side)

TBD

- [1] C1 channel – Pre-Driver output voltage, C4 channel – Current measured (scaled as 1A/1V, or 10mA/div).
 [2] Pre-driver output discharging 10nF capacitor.

Figure 5-19: Pre-Driver toggling at $V_{VBAT}=40V$

TBD

- [1] C1 channel – VCP, C2 channel – VPX, C3 channel – high-side gate output (OUT_HS), C4 channel – low-side gate output (OUT_LS), Function channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 5-20: Pre-Driver toggling at $V_{VBAT}=5.5V$

TBD

- [1] C1 channel – VCP, C2 channel – VPX, C3 channel – high-side gate output (OUT_HS), C4 channel – low-side gate output (OUT_LS), Function channel – VPX subtracted from high-side gate output (VGS of high-side FET).

Figure 5-21: Low-side propagation delay measurements (rising edge)

TBD

- [1] VBAT=12V. C4 channel – PWM command; C1 channel – low-side gate output.

Figure 5-22: Low-side propagation delay measurements (falling edge)

TBD

- [1] VBAT=12V. C4 channel – PWM command; C1 channel – low-side gate output.

Figure 5-23: High-side propagation delay measurements (rising edge)

TBD

- [1] VBAT=12V. C3 channel – PWM command; C2 channel – high-side gate output.

Figure 5-24: High-side propagation delay measurements (falling edge)

TBD

- [1] VBAT=12V. C3 channel – PWM command; C2 channel – high-side gate output.

Figure 5-25: Demonstration of -10V support for all phases toggling in-phase

TBD

- [1] C1/C2/C3 channel - high-side output for phases U/V/W toggling between -10V and approximately 0.5V; C4 channel - VCP.

Figure 5-26: Pre-Driver system response during VBAT power step (from 17V to 40V)

TBD

- [1] C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.
[2] All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

Figure 5-27: Pre-Driver system response during VBAT power step (from 40V to 17V)

TBD

- [1] C1 channel - VPX, C2 channel - VCP, C3 channel - VBAT, C4 channel - DVDD.
[2] All phases are toggling in phase. The power is switched between 17V to 40V with 1.2MV/s slew rate.

Figure 5-28: Pre-Driver system response during VBAT/VBATCP power step (from 12V to 24V)

TBD

- [1] C1/2/3 channel – VPX_U/V/W, C4 channel - VBATCP.
[2] All phases are toggling in phase. The power is switched between 12V to 24V with about 1MV/s slew rate.

Figure 5-29: H-bridge switching (using IRF640N FET's) when Pre-driver uses max current setting for each time segment

TBD

- [1] C1 – VCP, C2 – VPX, C3 – OUT_HS, C4 – OUT_LS, F1 – OUT_HS-VPX, i.e. V_{GS} of high-side FET.

Figure 5-30: H-bridge switching (using IRF640N FET's) when Pre-driver uses min current setting for each time segment

TBD

- [1] C1 – VCP, C2 – VPX, C3 – OUT_HS, C4 – OUT_LS, F1 – OUT_HS-VPX, i.e. V_{GS} of high-side FET.

5.22 LIN transceiver characteristics

Table 5-30: LIN receiver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
V _{BUS_REC}	Receiver recessive state	LIN SPEC 2.2 (Par. 18)	0.6	—	—	V _{VBAT}
V _{BUS_DOM}	Receiver dominant state	LIN SPEC 2.2 (Par. 17)	—	—	0.4	V _{VBAT}
V _{BUS_CNT}	Receiver center voltage	LIN SPEC 2.2 (Par. 19)	0.475	0.5	0.525	V _{VBAT}
V _{HYS}	Receiver hysteresis	LIN SPEC 2.2 (Par. 20)	0.07	0.12	0.175	V _{VBAT}
t _{RX_PD(L)}	Propagation delay bus dominant to RxD LOW	LIN Spec 2.2 (Par. 31)	0.1	—	6.0	us
t _{RX_PD(H)}	Propagation delay bus recessive to RxD HIGH	LIN Spec 2.2 (Par. 31)	0.1	—	6.0	us
t _{RX_SYM}	Receiver delay symmetry	t _{RX_SYM} = t _{RX_PD(L)} - t _{RX_PD(H)} LIN Spec 2.2 (Par. 32)	-2.0	—	2.0	us

Table 5-31: LIN wake-up characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
V _{TH_WK}	Wake-up threshold	T _J = -40 ~ 150 °C	0.475	0.52	0.55	V _{VBAT}
V _{TH_WK_HYST}	Wake-up hysteresis	T _J = -40 ~ 150 °C	0.04	0.07	0.10	V _{VBAT}
t _{WK_FILT_ANA} ^[1]	Wake-up filter time (internal analog filter delay)	—	—	3.83	—	us

[1] The total dominant time for LIN wake-up is t_{WK_FILT_ANA} plus digital filter time (>100us).

Table 5-32: LIN transmitter characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
V _{BUS_REC_OUT}	Bus recessive output voltage	5.5V ≤ V _{VBAT} ≤ 28V	0.8	—	—	V _{VBAT}
V _{BUS_DOM_OUT}	Bus dominant output voltage	7V ≤ V _{VBAT} ≤ 28V	—	—	0.2	V _{VBAT}
		5.5V ≤ V _{VBAT} < 7V	—	—	0.223	V _{VBAT}
I _{BUS_LIM}	Bus short circuit current	LIN Spec 2.2 (Par. 12)	40.0	—	100.0	mA
t _{BUS_Short_filt}	Bus short circuit filter time	—	—	9	—	us
I _{BUS_NO_GND} ^[1]	Leakage current (loss of ground)	LIN Spec 2.2 (Par. 15)	-1000	-425.8	1000	uA
I _{BUS_NO_BAT}	Leakage current	LIN Spec 2.2 (Par. 16)	—	10.6	22.0	uA
I _{BUS_PAS_dom}	Leakage current	LIN Spec 2.2 (Par. 13)	-1.0	-0.545	—	mA
I _{BUS_PAS_rec}	Leakage current	LIN Spec 2.2 (Par. 14)	—	6.23	20.0	uA
R _{slave}	Bus pull-up resistance	LIN Spec 2.2 (Par. 26)	20.0	32.3	47.0	kΩ
D1 ^[2]	Duty cycle D1 Normal Slope Mode	LIN Spec 2.2 (Par. 27) 1K pull-up resistor	0.396	—	—	—

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	(for worst case at 20 kbit/s)	1nF load cap or 0.5K pull-up resistor 10nF load cap				
D2 ^[3]	Duty cycle D2 Normal Slope Mode (for worst case at 20 kbit/s)	LIN Spec 2.2 (Par. 28) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	–	–	0.581	–
D3 ^[4]	Duty cycle D3 (for worst case at 10.4 kbit/s)	LIN Spec 2.2 (Par. 29) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	0.417	–	–	–
D4 ^[5]	Duty cycle D4 (for worst case at 10.4 kbit/s)	LIN Spec 2.2 (Par. 30) 1K pull-up resistor 1nF load cap or 0.5K pull-up resistor 10nF load cap	–	–	0.590	–
D5 ^{[1][6][8]}	Duty cycle D5 (for worst case at 115 kbit/s) for +1 μ s Receiver delay symmetry	0.5K pull-up resistor 1nF load cap	0.350	–	–	–
D6 ^{[1][7][8]}	Duty cycle D6 (for worst case at 115 kbit/s) for +1 μ s Receiver delay symmetry	0.5K pull-up resistor 1nF load cap	–	–	0.700	–
C _{LIN_IN}	LIN input capacity	–	–	15	30.0	pF
t _{timeout}	TxD dominant time out	V _{TxD} = 0 V	–	12.4	–	ms
T _{j_SD} ^[1]	Thermal shutdown temp	–	140	160	180	°C
DT ^[1]	Thermal shutdown hysteresis	–	–	10	–	°C

[1] Not subject to production test, guaranteed by design.

[2] THRec(max) = 0.744 $\times$ VS; THDom(max) = 0.581 $\times$ VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 50 μ s; D1 = tbus_rec(min)/2 tbit;

[3] THRec(min) = 0.422 $\times$ VS; THDom(min) = 0.284 $\times$ VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 50 μ s; D1 = tbus_rec(max)/2 tbit;

[4] THRec(max) = 0.778 $\times$ VS; THDom(max) = 0.616 $\times$ VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 96 μ s; D1 = tbus_rec(min)/2 tbit;

[5] THRec(min) = 0.389 $\times$ VS; THDom(min) = 0.251 $\times$ VS; V_{VBAT} = 5.5 ~ 18 V; tbit = 96 μ s; D1 = tbus_rec(max)/2 tbit;

[6] THRec(max) = 0.744 $\times$ VS; THDom(max) = 0.581 $\times$ VS; V_{VBAT} = 13.5 V; tbit = 13 μ s; D1 = tbus_rec(min)/2 tbit;

[7] THRec(min) = 0.422 $\times$ VS; THDom(min) = 0.284 $\times$ VS; V_{VBAT} = 13.5 V; tbit = 13 μ s; D1 = tbus_rec(max)/2 tbit.

[8] D5~D6 bus load condition is 0.5K pull-up resistor and 1nF load cap.

5.23 SPI characteristics

Table 5-33: SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	—	—	—	50	MHz
$t_{\text{SCLK(H)}}$	SCLK clock high time	—	10	—	—	ns
$t_{\text{SCLK(L)}}$	SCLK clock low time	—	10	—	—	ns
SPI master mode						
$t_{\text{V(MO)}}$	Data output valid time	—	—	—	9.5	ns
$t_{\text{H(MO)}}$	Data output hold time	—	3.9	—	—	ns
$t_{\text{SU(MI)}}$	Data input setup time	—	6	—	—	ns
$t_{\text{H(MI)}}$	Data input hold time	—	2	—	—	ns
SPI slave mode						
$t_{\text{SU(SFRM)}}$	SFRM enable setup time	—	5.6	—	—	ns
$t_{\text{H(SFRM)}}$	SFRM enable hold time	—	1.5	—	—	ns
$t_{\text{A(SO)}}$	Data output access time	—	4	—	10	ns
$t_{\text{DIS(SO)}}$	Data output disable time	—	4	—	10	ns
$t_{\text{V(SO)}}$	Data output valid time	—	—	—	9.5	ns
$t_{\text{H(SO)}}$	Data output hold time	—	3.9	—	—	ns
$t_{\text{SU(SI)}}$	Data input setup time	—	6	—	—	ns
$t_{\text{H(SI)}}$	Data input hold time	—	2	—	—	ns

5.24 MON characteristics

Table 5-34: MON characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
$V_{TH}^{[1]}$	Wake-up/monitoring threshold voltage	—	0.48	0.50	0.53	V_{VBAT}
$V_{TH_HYST}^{[1]}$	Threshold hysteresis	—	0.04	0.065	0.08	V_{VBAT}
I_{PU}	Pull-up current	$0.6 * V_{VBAT}$	-20	-10	-1	μA
I_{PD}	Pull-down current	$0.4 * V_{VBAT}$	1	10	20	μA
I_{IK}	Input leakage current	$0V < V_{MON} < 28V$ $5.5V < V_{VBAT} < 28V$	-2	—	2	μA
I_{on}	Operation current	$T_J = -40 \sim 150\text{ }^{\circ}C$	—	1.7	4	μA
$I_{off}^{[2]}$	Off current	—	—	10	300	nA
$t_{WK_FILT_ANA}^{[3]}$	Wake-up filter time (internal analog filter delay)	—	—	3.55	—	μs

[1] Without external serial resistor R_s (with R_s : $\Delta V = I_{PD} * R_s$ or $\Delta V = I_{PU} * R_s$).

[2] Not subject to production test, guaranteed by design.

[3] The minimal time for MON wake-up is $t_{WK_FILT_ANA}$ plus digital filter time (>50 μs).

5.25 DVDD5 characteristics

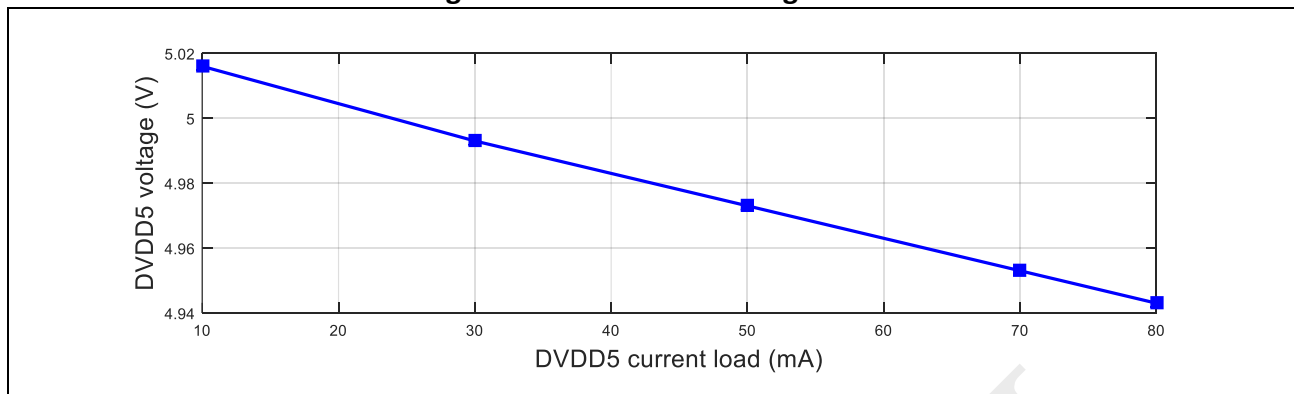
Table 5-35: DVDD5 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
$C_{load}^{[1]}$	Load capacitor	—	2.2	—	4.7	μF
I_{load}	Load current @ active mode	—	—	—	90	mA
V_{out_trim}	Trim step @ active mode	—	—	66.67	—	mV
V_{out}	Output voltage @ active mode	—	—	5	—	V
dV_{load}	Load regulation @ active mode	—	—	68	250	mV
I_{oc}	Overcurrent threshold @ active mode	—	81	151	312	mA
$V_{out}^{[2]}$	Output voltage @ stop mode	—	—	5	—	V

[1] Not subject to production test, guaranteed by design.

[2] Only drive internal loading.

Figure 5-31: DVDD5 load regulation



5.26 DVDD33 characteristics

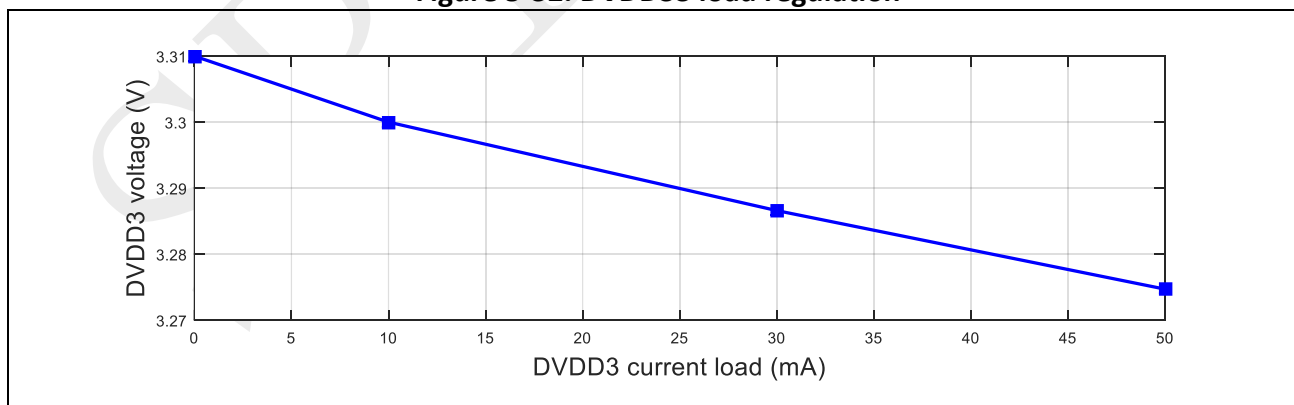
Table 5-36: DVDD33 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
$C_{load}^{[1]}$	Load capacitor	—	2.2	—	4.7	uF
I_{load}	Load current @ active mode	—	—	—	60	mA
V_{out_trim}	Trim step @ active mode	—	—	44	—	mV
V_{out}	Output voltage @ active mode	—	—	3.3	—	V
dV_{load}	Load regulation @ active mode	—	—	38.65	66	mV
I_{oc}	Overcurrent threshold @ active mode	—	75	95	115	mA
$V_{out}^{[2]}$	Output voltage @ stop mode	—	—	3.3	—	V

[1] Not subject to production test, guaranteed by design.

[2] Only internal current.

Figure 5-32: DVDD33 load regulation



5.27 VCAP12 characteristics

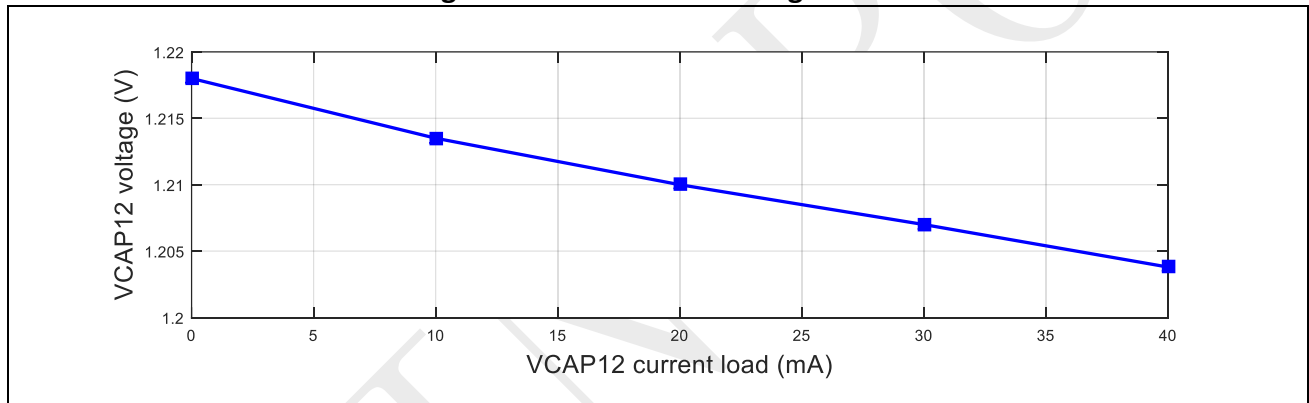
Table 5-37: VCAP12 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	—	5.5	—	28	V
	Extend power supply range	—	28	—	40	V
$C_{load}^{[1]}$	Load capacitor	—	1	2.2	4.7	uF
I_{load}	Load current @ active mode	—	—	—	40	mA
V_{out_trim}	Trim step @ active mode	—	—	20	—	mV
V_{out}	Output voltage @ active mode	—	—	1.2	—	V
dV_{load}	Load regulation @ active mode	—	—	14	40	mV
I_{oc}	Overcurrent threshold @ active mode	—	60	81.5	107	mA
$V_{out}^{[2]}$	Output voltage @ stop mode	—	—	1.2	—	V

[1] Not subject to production test, guaranteed by design.

[2] Only internal current.

Figure 5-33: VCAP12 load regulation



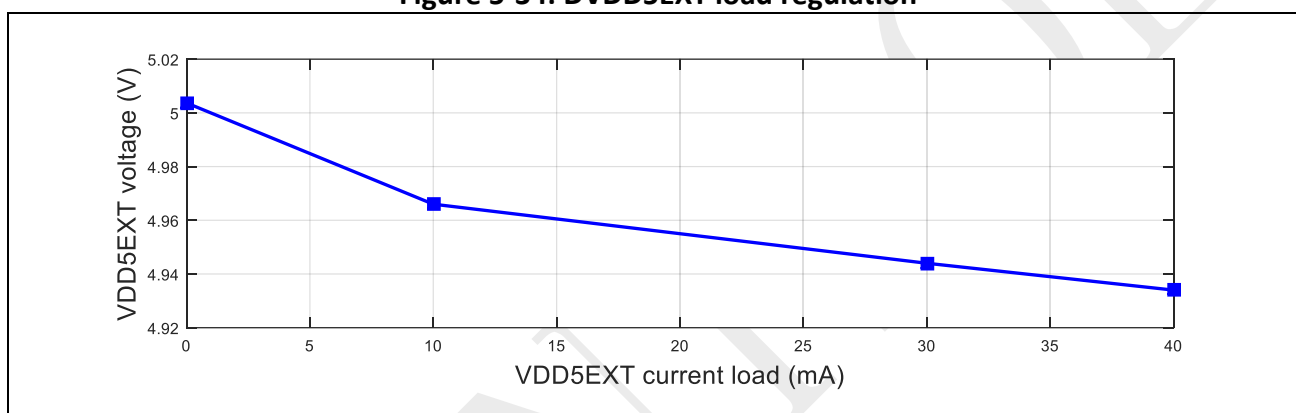
5.28 DVDD5EXT characteristics

Table 5-38: DVDD5EXT characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBAT}	Power supply	—	5.5	—	28	V
$C_{load}^{[1]}$	Load capacitor	—	1	2.2	4.7	μF
I_{load}	Load current @ active mode	—	—	—	40	mA
V_{out_trim}	Trim step @ active mode	—	—	66.67	—	mV
V_{out}	Output voltage @ active mode	—	—	5	—	V
dV_{load}	Load regulation @ active mode	—	—	69.7	123	mV
I_{oc}	Overcurrent threshold @ active mode	—	45	77.33	170	mA

[1] Not subject to production test, guaranteed by design.

Figure 5-34: DVDD5EXT load regulation



5.29 Flash memory characteristics

The characteristics are given at $T_J = -40$ to $150\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 5-39: Flash memory characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{RD}	Read access time	—	35	—	ns
t_{PROG}	Word (64-bit) program time	—	8	10	μs
t_{SE}	Sector erase time	—	3.2	4	ms
t_{CE}	Chip erase time	—	16	20	ms
N_{END}	Endurance (erase/program cycle)	$T_J = 85\text{ }^{\circ}\text{C}$	100,000	—	cycles
t_{RET}	Data retention duration	$T_J = 85\text{ }^{\circ}\text{C}$	20	—	years

5.30 Electrical sensitivity characteristics

Table 5-40: ESD absolute maximum ratings (TBD)

Symbol	Parameter	Conditions		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature $T_A = 25\text{ }^{\circ}\text{C}$	LIN Pin	8000	V
			VBAT Pin VBATM Pin VBATCP Pin MON Pin	4000	V
			Other Pins	2000	V
			—	500	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature $T_A = 25\text{ }^{\circ}\text{C}$	—	500	V
			Corner Pins	750	V

Table 5-41: Electrical sensitivities (TBD)

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	Ambient temperature $T_A = 125\text{ }^{\circ}\text{C}$ $V_{VBAT}=V_{VBATM}=V_{VBATCP}=40\text{V}$, $V_{DVDD5} = 5.5\text{V}$, $V_{DVDD33} = 3.63\text{V}$, $V_{VCAP12} = 1.32\text{V}$	100	mA

5.31 Moisture Sensitivity Level characteristics

Table 5-42: Thermal resistance characteristics (QFN48 package) (TBD)

Symbol	Parameter	Conditions	Max	Unit
MSL	Moisture Sensitivity Level	—	3	—

5.32 Thermal resistance characteristics

Table 5-43: Thermal resistance characteristics (QFN48 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	—	5.4751	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Junction-to-ambient thermal resistance	2-layer PCB ^[1] PCB Copper content (Top layer = 60%, Bottom layer = 80%)	28.0204	$^{\circ}\text{C}/\text{W}$

[1] The size of PCB test board is 110mm x 110mm x 1.6mm.

Table 5-44: Thermal resistance characteristics (QFN56 package)

Symbol	Parameter	Conditions	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	—	6.5942	$^{\circ}\text{C}/\text{W}$
θ_{JA}	Junction-to-ambient thermal resistance	4-layer PCB ^[1] PCB Copper content (Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%)	27.9046	$^{\circ}\text{C}/\text{W}$

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

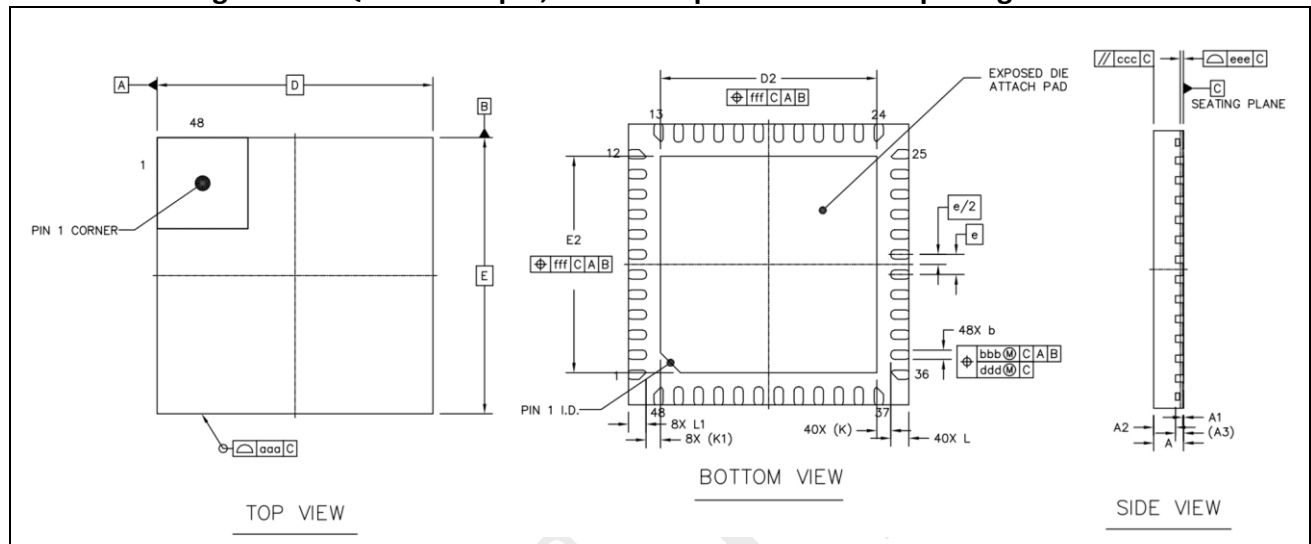
6 Package information

The package type of SPD1177 is 48-pin QFN or 56-pin QFN. The detail information is as follows:

6.1 QFN48

6.1.1 Package Specification

Figure 6-1: QFN48 – 48 pin, 7 x 7 mm quad flat no-lead package outline



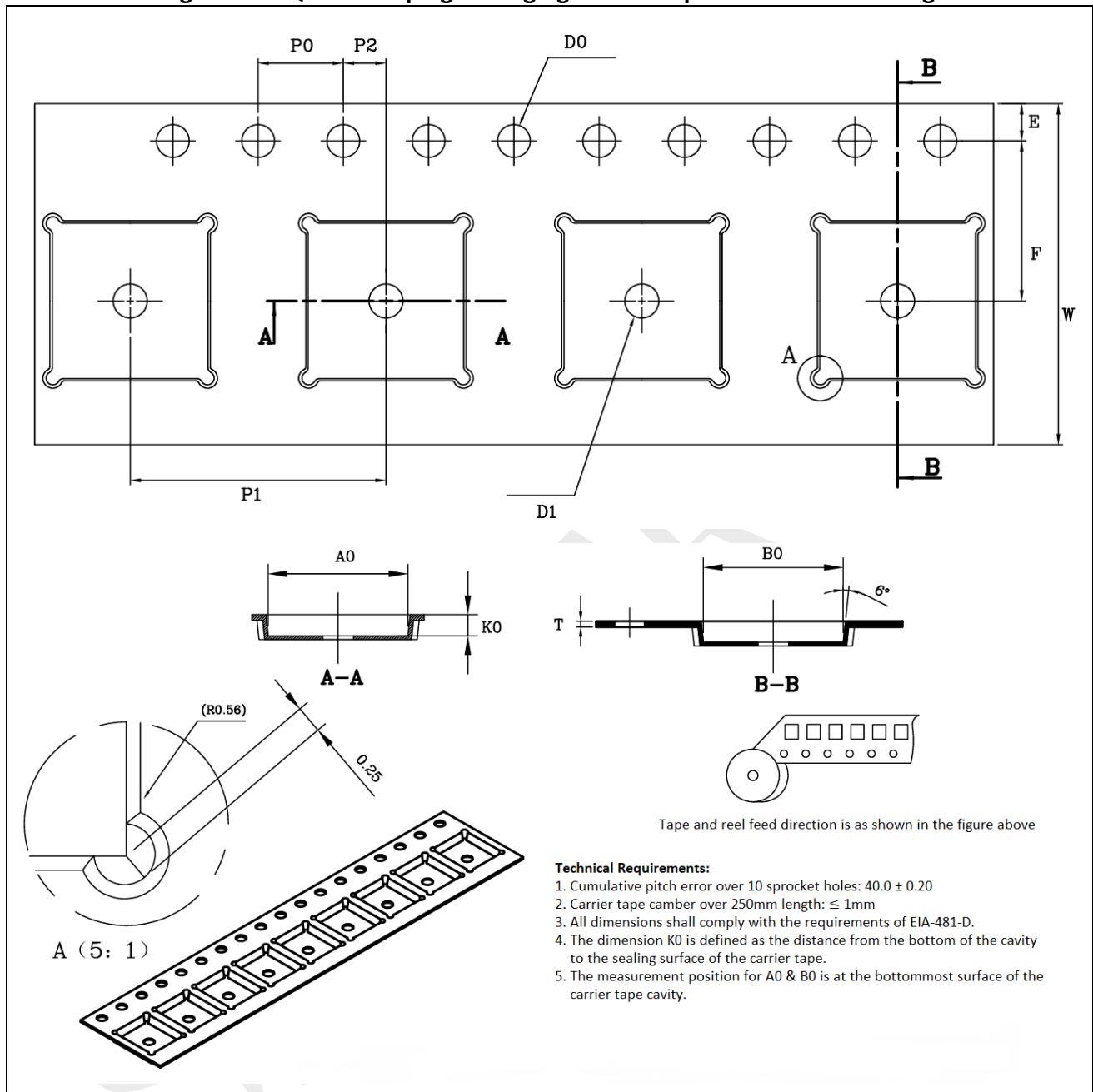
[1] Drawing is not to scale.s

Table 6-1: QFN48 – 48 pin, 7 x 7 mm quad flat no-lead package mechanical data

Description		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	—	0.55	—
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D	7 BSC		
	Y	E	7 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	5.3	5.4	5.5
	Y	E2	5.3	5.4	5.5
LEAD LENGTH		L	0.35	0.45	0.55
		L1	0.34	0.44	0.54
LEAD TIP TO EXPOSED PAD EDGE		K	0.35 REF		
		K1	0.36 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
		ddd	0.05		
EXPOSED PAD OFFSET		fff	0.1		

6.1.2 Packing Specification

Figure 6-2: QFN7*7 Taping Packaging Carrier Tape Dimension Drawing



[1] Drawing is not to scale.

Table 6-2: Taping Packaging Dimension

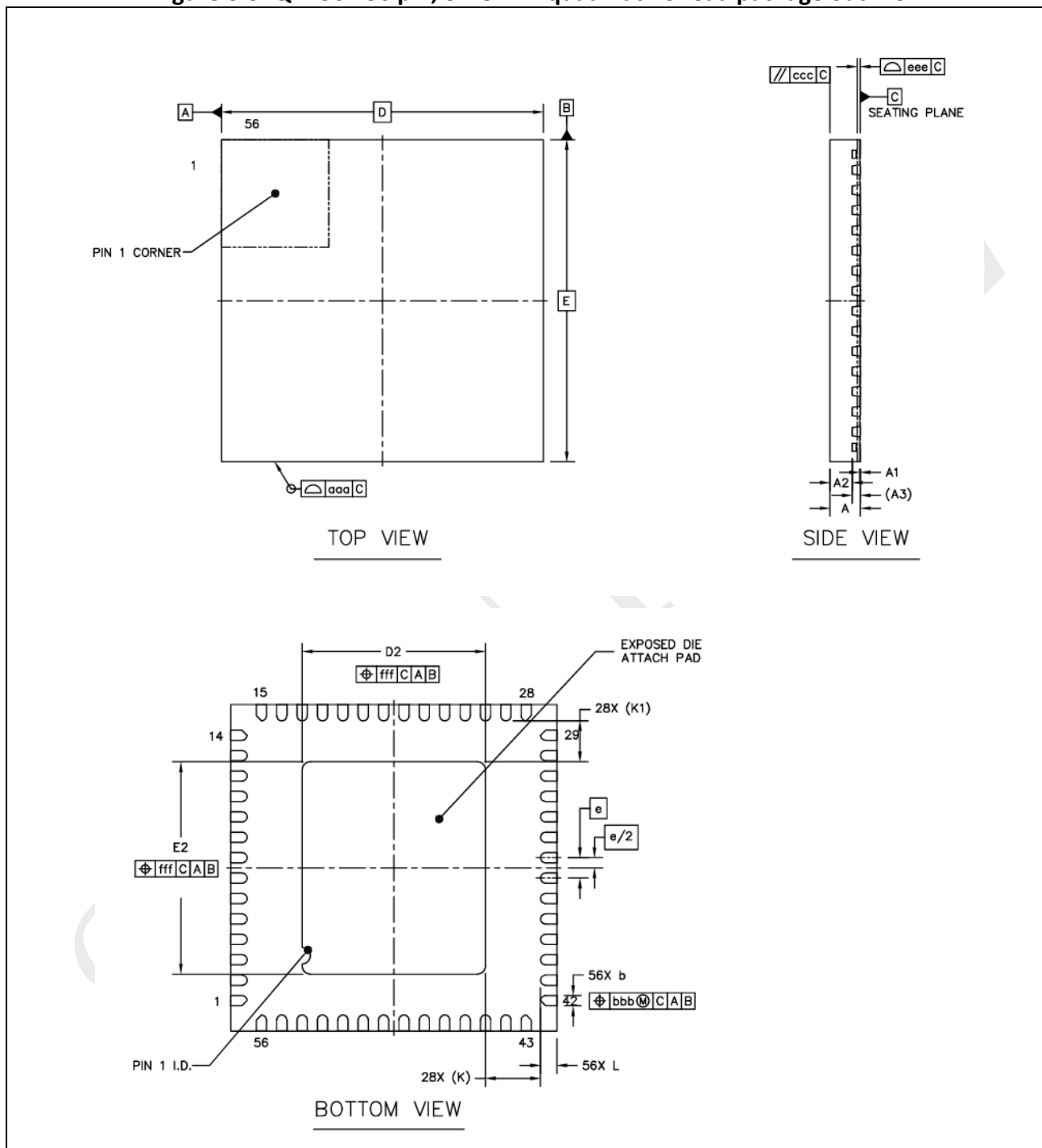
Spec.	A0	B0	K0	D0	D1	W	E	F	P0	P1	P2	T
Dim.	7.30 ± 0.10	7.30 ± 0.10	1.10 ± 0.10	1.50 $+0.10$ 0.00	1.50 $+0.25$ 0.00	16.00 ± 0.30	1.75 ± 0.10	7.50 ± 0.10	4.00 ± 0.10	12.00 ± 0.10	2.00 ± 0.10	0.30 ± 0.05

[1] Surface Impedance: $10^5 - 10^9 \Omega$

6.2 QFN56

6.2.1 Package Specification

Figure 6-3: QFN56 - 56 pin, 8 x 8 mm quad flat no-lead package outline



[1] Drawing is not to scale.

[2] The package mechanical data may be adjusted in future.

Table 6-3: QFN56 - 56 pin, 8 x 8 mm quad flat no-lead package mechanical data

Description		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	—	0.55	—
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D	8 BSC		
	Y	E	8 BSC		
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D2	4.4	4.5	4.6
	Y	E2	5.1	5.2	5.3
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	1.35 REF		
		K1	1 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.1		
EXPOSED PAD OFFSET		fff	0.1		

7 Ordering information

Table 7-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Pre-Driver	Package	Grade	SPQ ^[1]	Packing
SPD1177API48	128KB	32KB	100MHz	3 Phase	QFN48	Industrial	3000	Reel
SPD1177API56	128KB	32KB	100MHz	3 Phase	QFN56	Industrial	3000	Reel

[1] SPQ = Standard Pack Quantity.

7.1 Rule of ordering number

Figure 7-1: Rule of ordering number

